Schematic Organization

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Sheet 03: LAYOUT Flow Diagram
Sheet 04: Power in Regulator
Sheet 05: FPGA Power
Sheet 06: FPGA & EPCS Configuration
Sheet 07: FPGA Banks 1,2,3,4
Sheet 08: FPGA Banks 5,6,7,8
Sheet 09: SRAM & QUSB Interface
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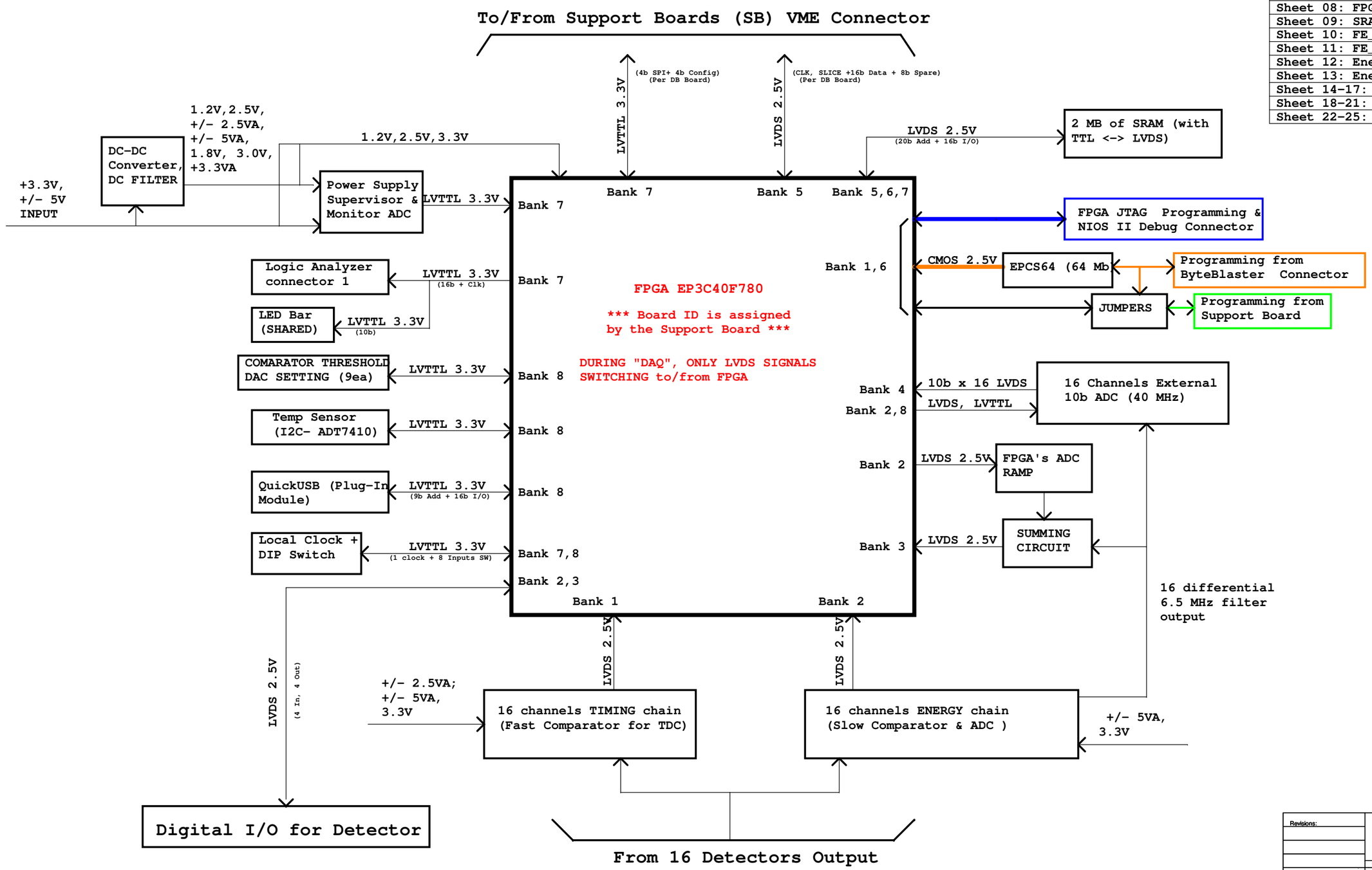
Sheet 11: FE_DACs
Sheet 12: Energy_External_ADC
Sheet 13: Energy_FPGA_ADC
Sheet 14-17: 4 Channels Fast Timing (Timing)
Sheet 18-21: 4 Channels Input Block
Sheet 22-25: 4 Channels Slow Timing (Energy)



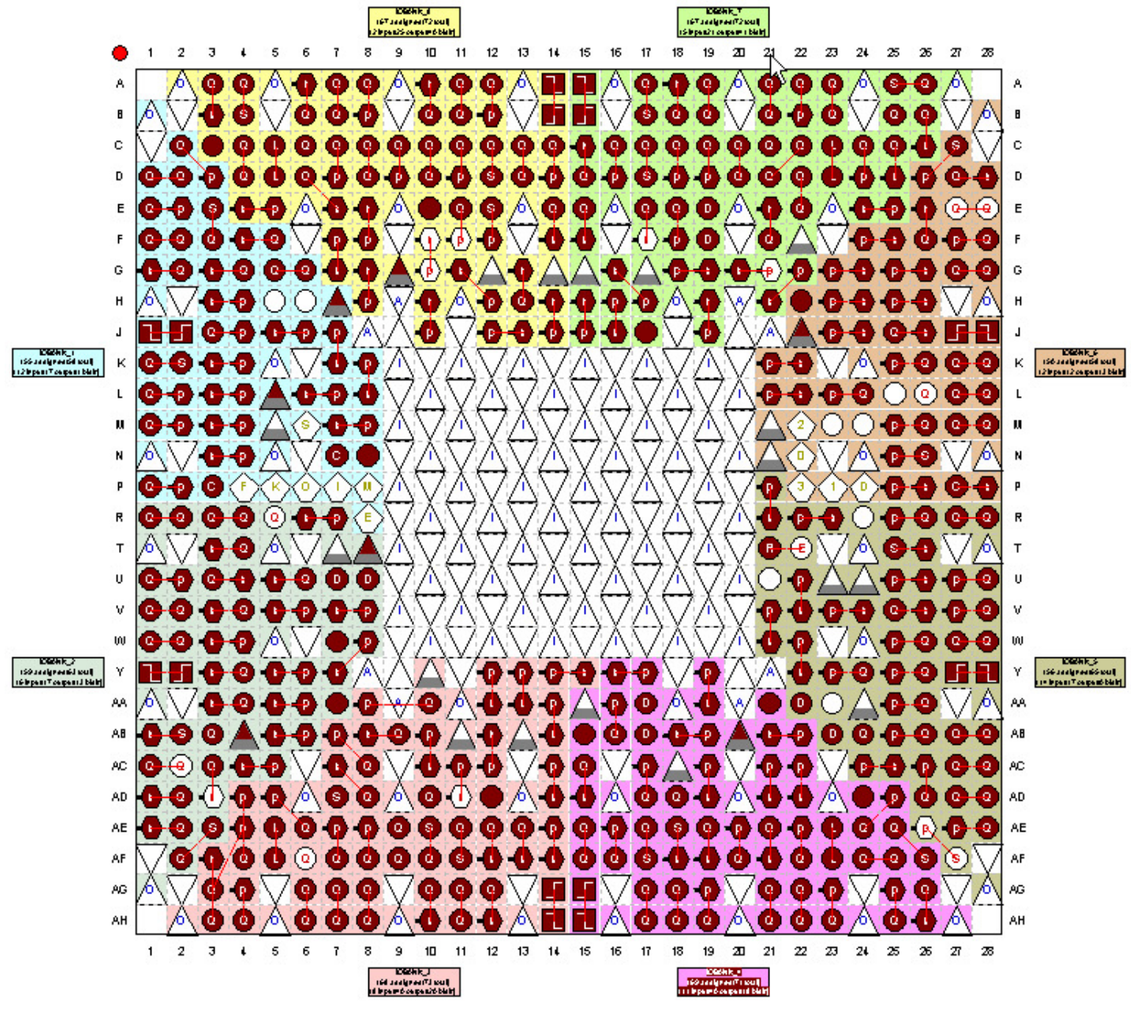
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL FAST TIMIN
Engineer: Chinh Vu	Title: **Title Block Diagram**
Designer: Judy Stirickinen	Project: **OPENPET- FAST DETECTOR BOARD**
DWG NO.: <Doc>	Size C · Modify Date: Wednesday, December 18, 2013 · Sheet 1 of 25 · Rev 0

Notes:

TYPICAL Cyclone III FPGA Package Top

BANK 8 BANK 7

Cyclone III - EP3C120F780C7



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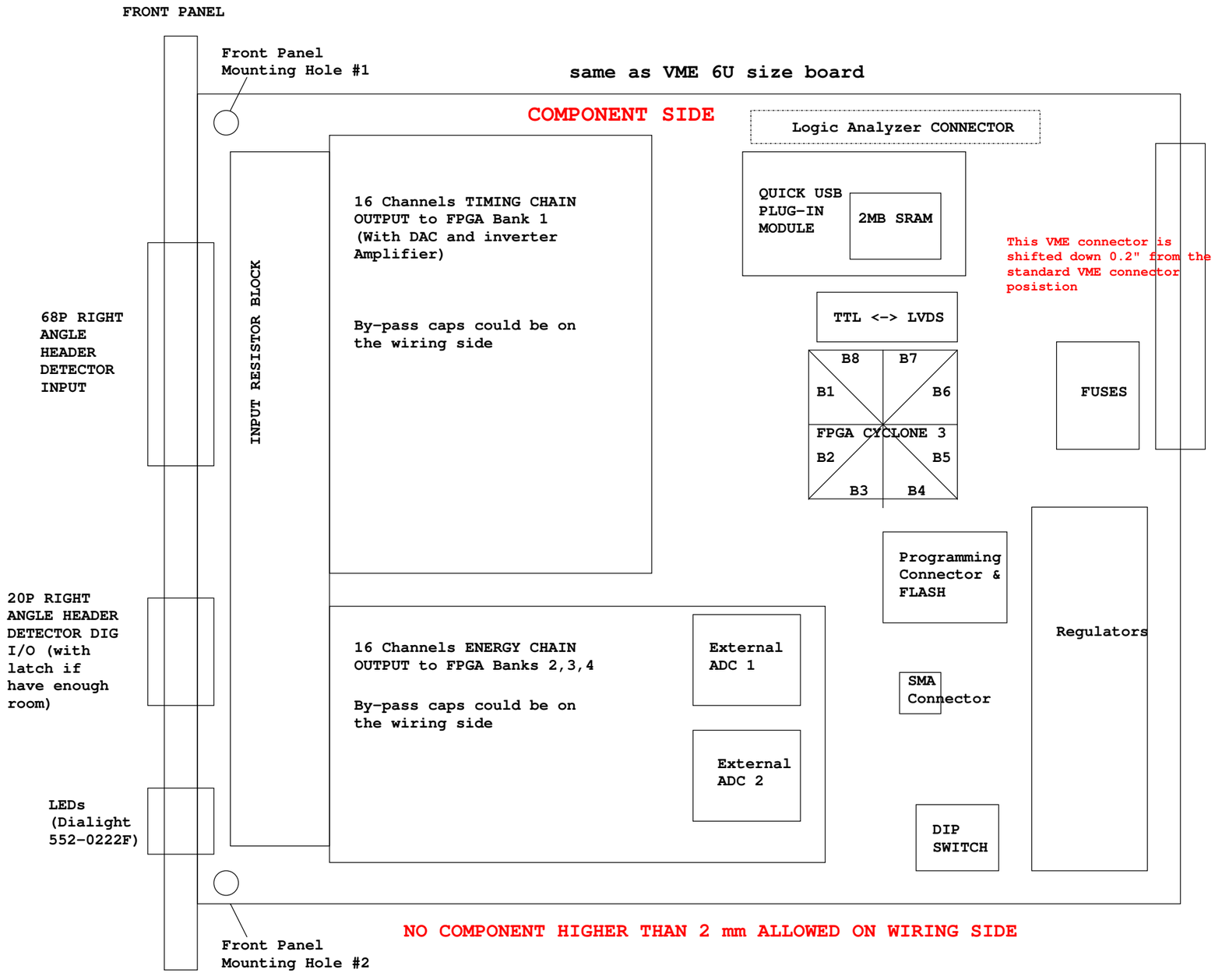
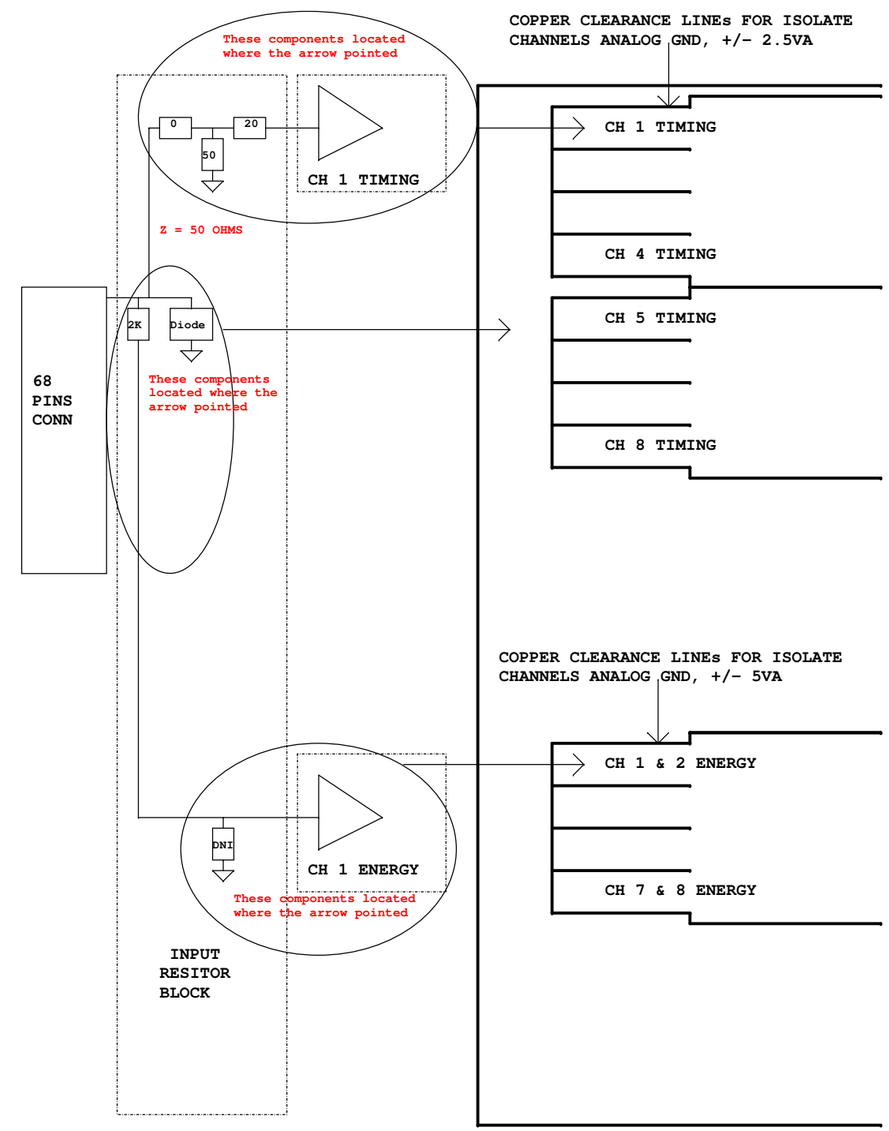
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL FAST TIMIN	
Engineer: Chinh Vu	Title: FPGA Package TOP	
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD	
DWG NO.: <Doc>	Size C / Modify Date: Wednesday, December 18, 2013	Sheet 2 of 25 / Rev 0

MAKE SURE TO HAVE (0.05") 50 Mils CLEARANCE FROM
THE PCB EDGE to the EDGE of ANY VIA PADs



NO COMPONENT HIGHER THAN 2 mm ALLOWED ON WIRING SIDE

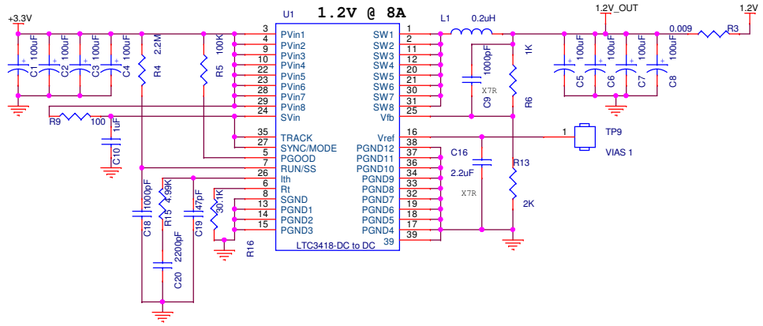
TYPICAL LAYOUT ONE OF 16 ANALOG INPUT CHANNELS



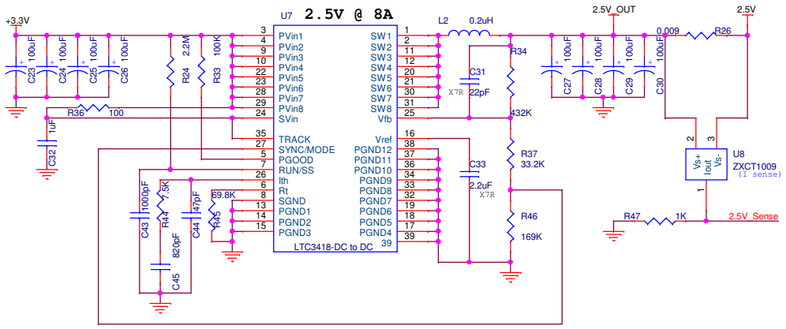
Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL FAST TIMIN
Engineer: Chinh Vu	Title: Layout Flow Diagram
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD
DWG NO.: <Doc>	Size C · Modify Date: Wednesday, December 18, 2013 · Sheet 3 of 25 · Rev 0

No need of special power up sequence for Cyclone 3 (page 249 of 350 Handbook)

POWER FOR FPGAs CORE



POWER FOR FPGAs I/O LVDS BANKs



*** For LTC3418-DC to DC ***

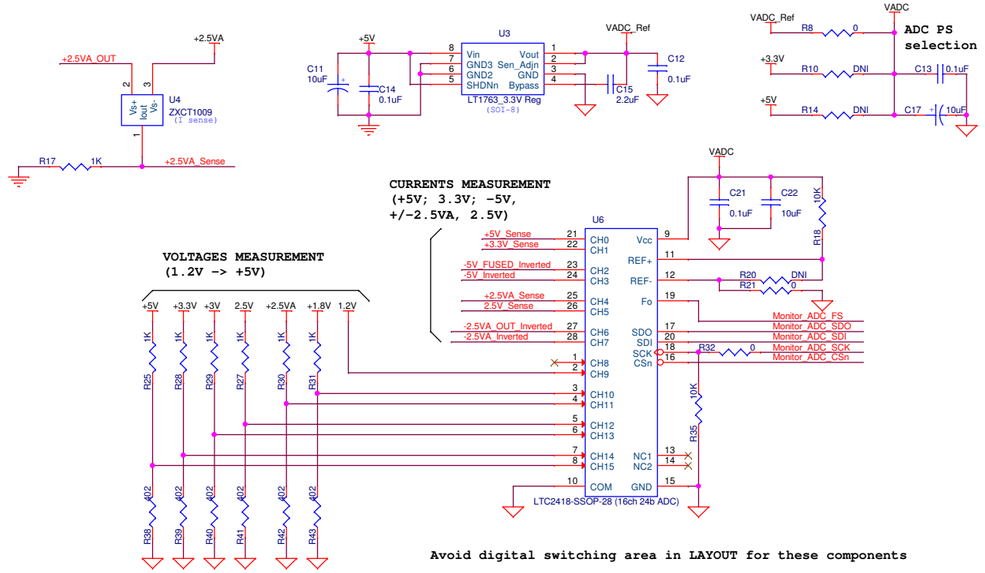
Use TDK C3225X5R0J107M for Tantatum
Use VISHAY DALE IHLP-2525CZ-01 for Inductor L
Use XR7 for ceramic cap

FPGA POWER SUPPLY

These TP will be distributed accross the board and label DGND

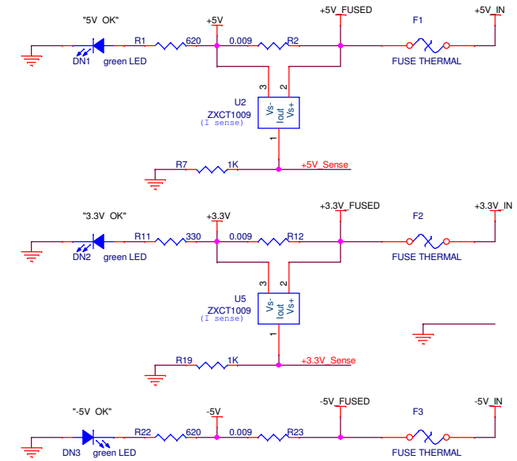
These TP will be distributed accross the board and label AGND

VOLTAGE and CURRENT SLOW MONITORING

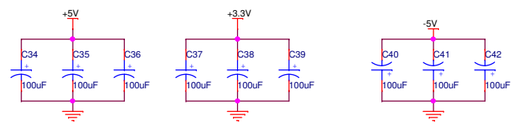


Avoid digital switching area in LAYOUT for these components

POWER to the BOARD from 96 pins Connector

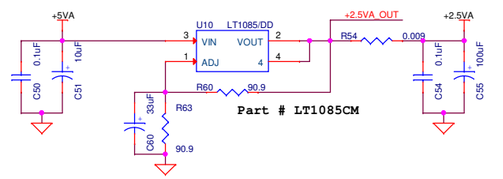


ADD the inverter to monitor the NEGATIVE V
the ZXCT1009 CAN NOT MONITOR I WITH V <= 2.5V
ADD OTHER MONITOR V & I

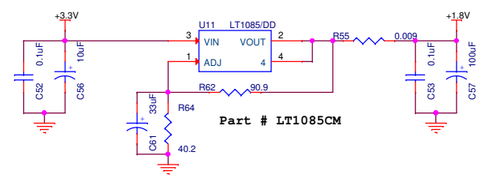


F.E. ANALOG SECTION REGULATORS and FILTERS

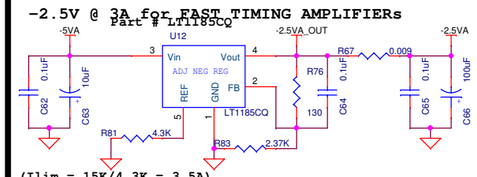
2.5V @ 3A for FAST TIMING AMPLIFIERs



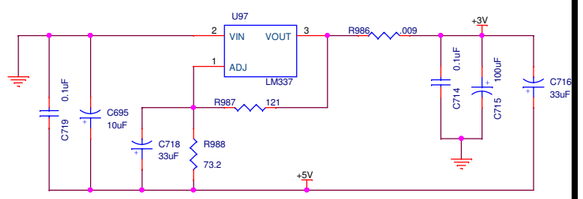
1.8V @ 3A for External ADC Digital



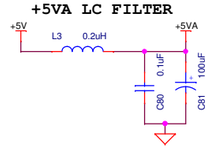
-2.5V @ 3A for FAST TIMING AMPLIFIERs



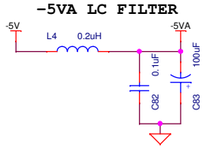
3V @ 3A for LVPECL Termination



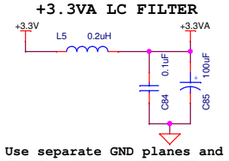
+5VA LC FILTER



-5VA LC FILTER

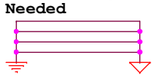


+3.3VA LC FILTER

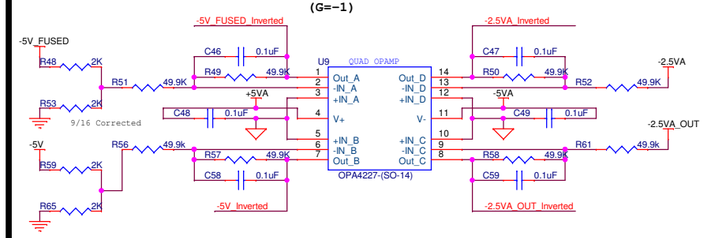


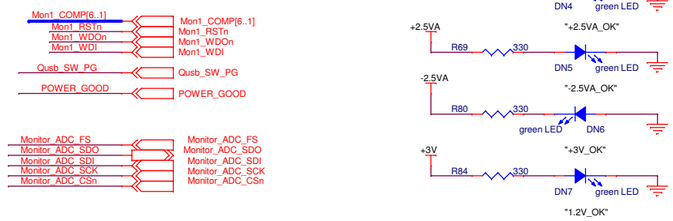
Use separate GND planes and CONNECT THESE 2 GROUNDs TOGETHER "HEAVILY" ONLY AT THE VME 96 PINS CONNECTOR

To control regulator if Needed

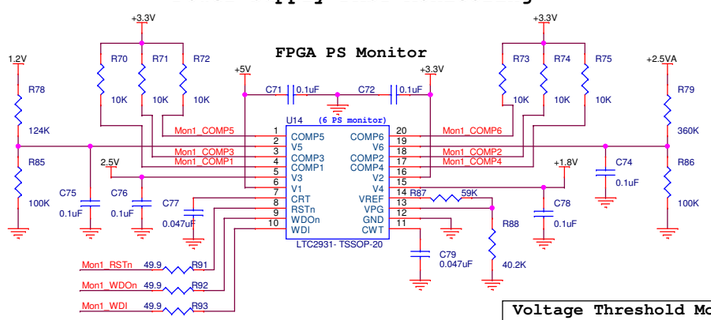


INVERTING AMPLIFIER (G=-1)





Power Supply FAST Monitoring



Voltage Threshold Mode 6

V1 (5.0V) Trip @ ~4.750V
V2 (3.3V) Trip @ ~3.135V
V3 (2.5V) Trip @ ~2.375V
V4 (1.8v) Trip @ ~1.710V
V5 (1.2V) Trip @ ~1.120V
V6 (2.5VAV) Trip @ ~2.375V

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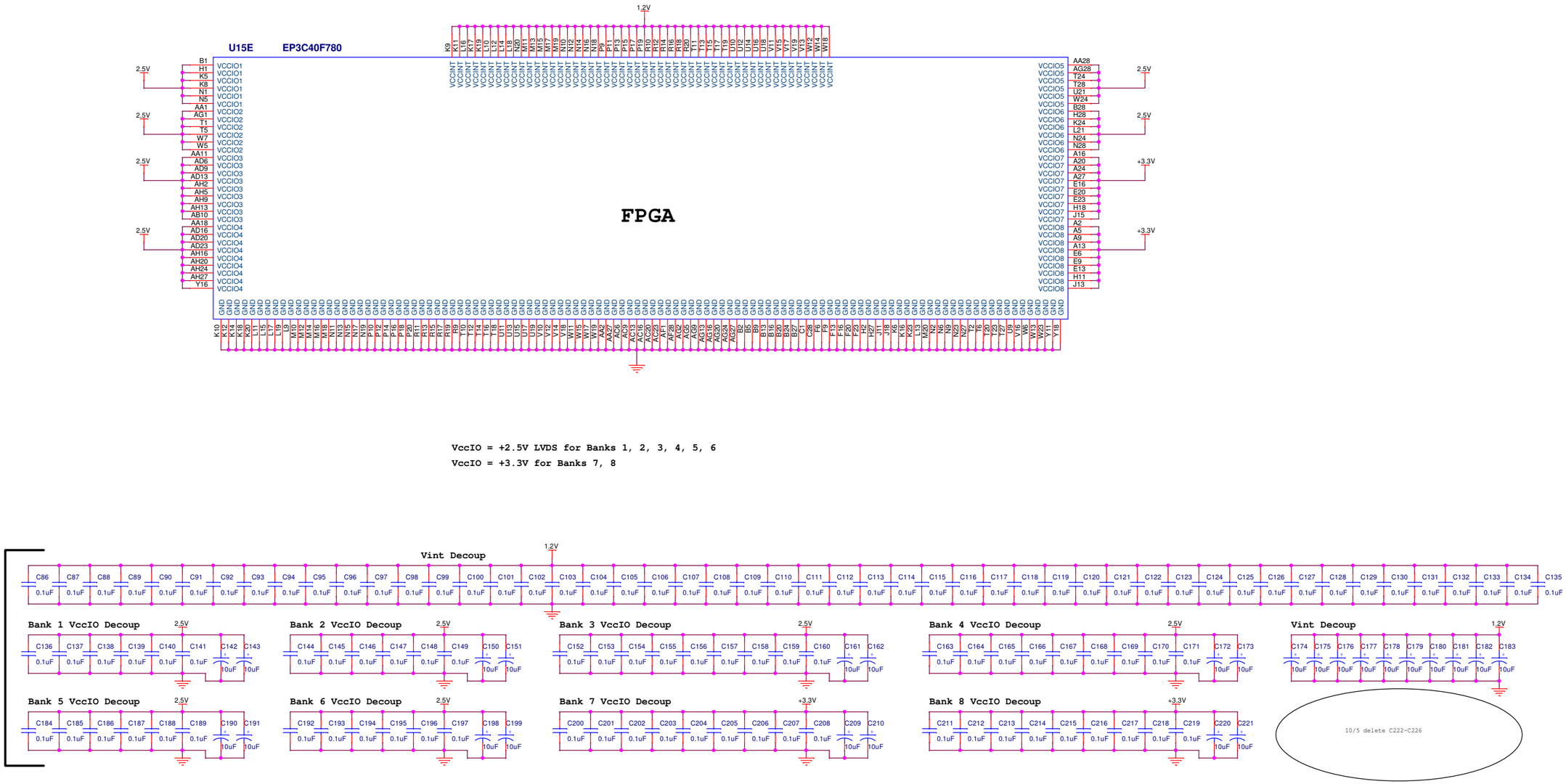
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL.F
Engineer: Chinh Vu	Title: Power In Regulator
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD
DWG NO.: <Doc>	Size C · Modify Date: Tuesday, January 07, 2014 · Sheet 4 of 25 · Rev 0



VccIO = +2.5V LVDS for Banks 1, 2, 3, 4, 5, 6

VccIO = +3.3V for Banks 7, 8

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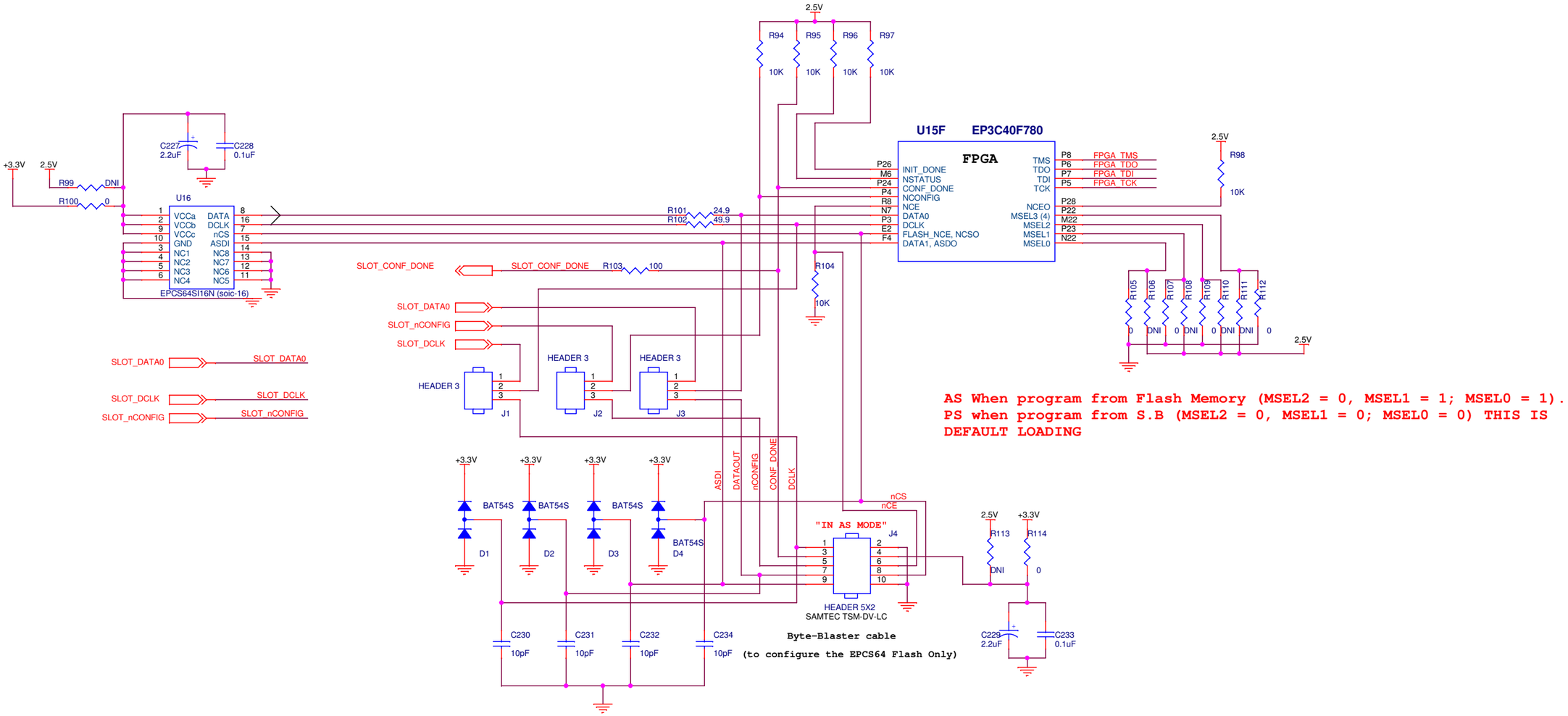
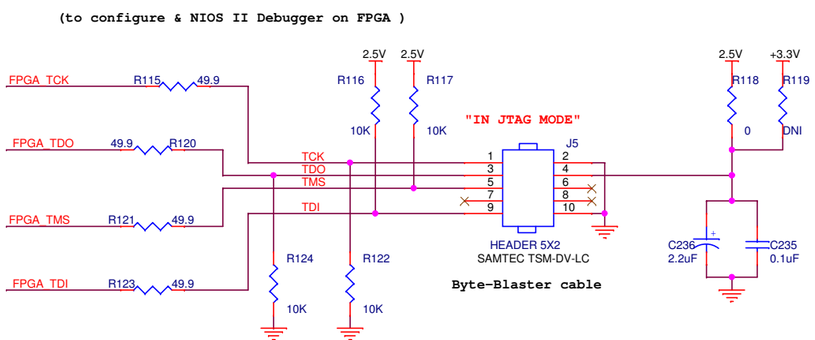
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL FAST TIMIN
Engineer: Chinh Vu	Title: FPGA POWER
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD
DWG NO.: <Doc>	Size C · Modify Date: Wednesday, December 18, 2013 · Sheet 5 of 25 · Rev 0





Configuration notes:

1) The EPCS64 Flash can be programmed in AS mode by only one way:

a) By Plug-in the Byte_Blaster cable to J9 from Host PC and set appropriate jumpers

2) The FPGA can be programmed either by

a) By Plug-in the Byte_Blaster cable to J9 from Host PC and set appropriate jumpers

a) By the S.B and set appropriate jumpers

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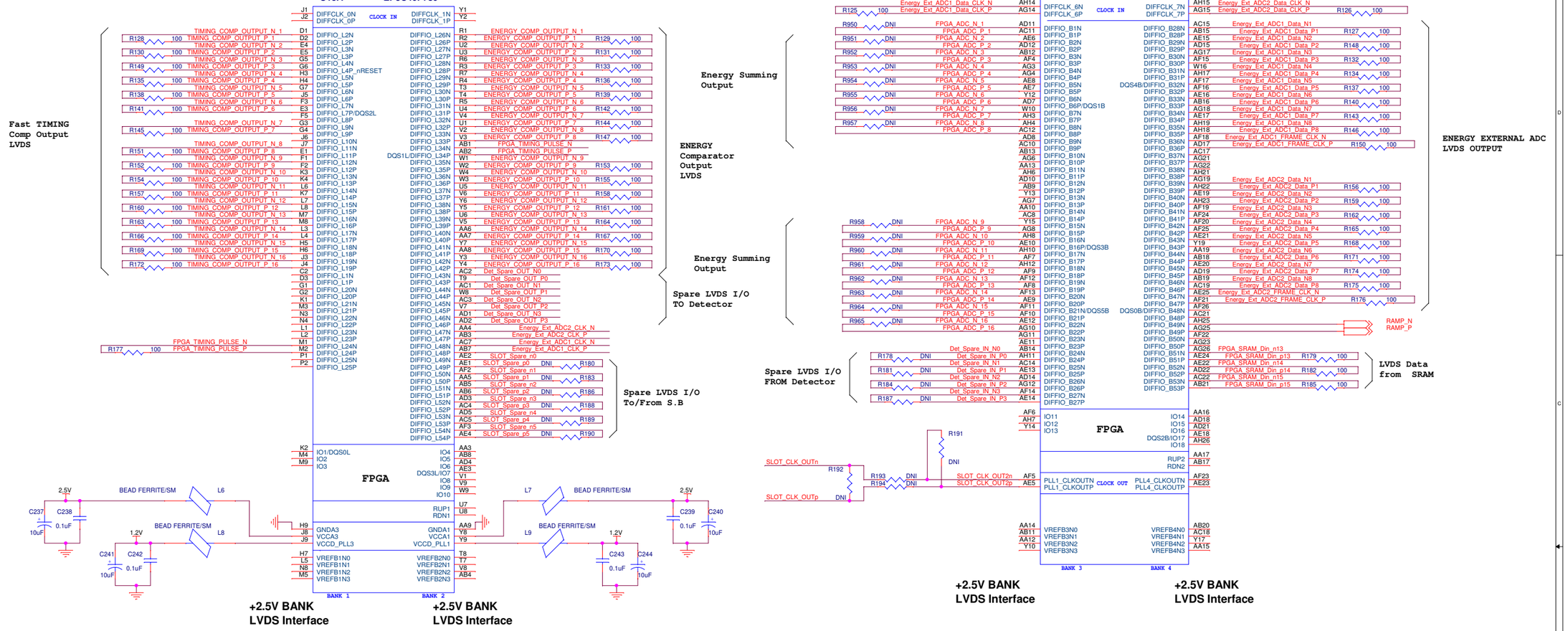
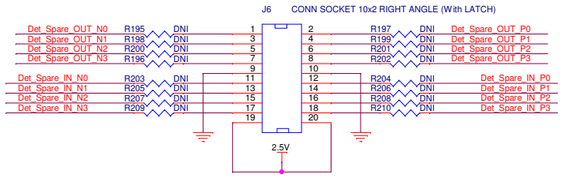
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL F
Engineer: Chinh Vu	Title: FPGA Configuration
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD
DWG NO.: <Doc>	Size D · Modify Date: Wednesday, December 18, 2013 · Sheet 6 of 25 · Rev 0



Digital LVDS I/O To/From Detector



EXTERNAL_ADC1_INTERFACE

EXTERNAL_ADC1_INTERFACE

LVDS DATA FROM SRAM

LVDS CLK to SLOT CONNECTOR

100 ohms required for LVDS reveivers. Pages 120,132/350 of Cyclone3_handbook.pdf

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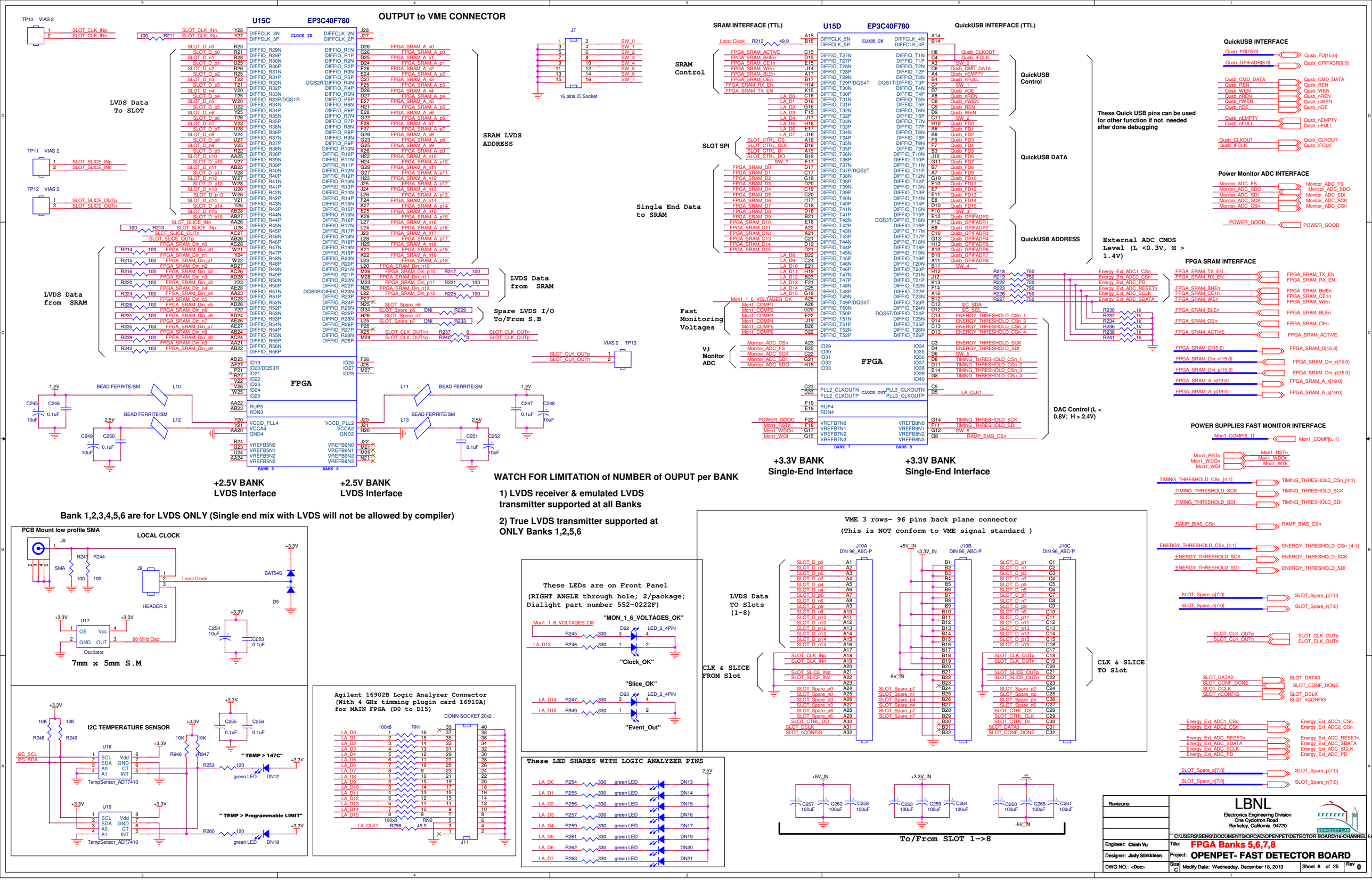
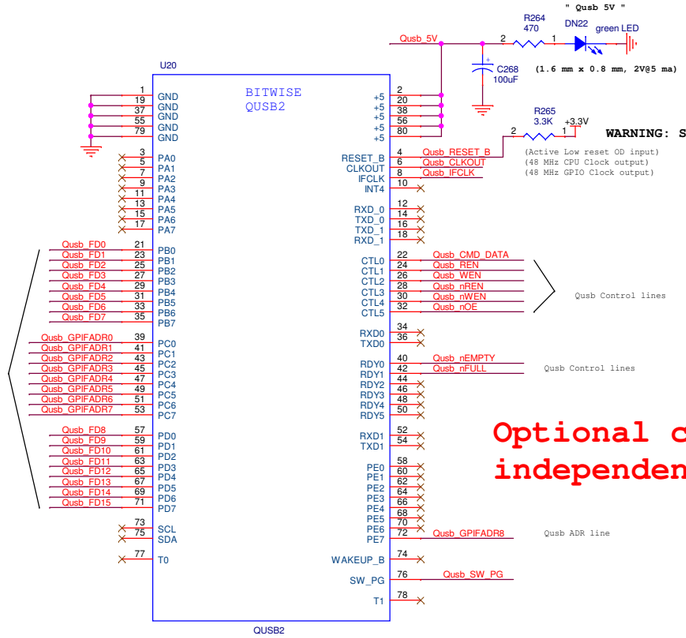
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL FAST
Engineer: Chinh Vu	Title: 07-FPGA_Banks_1,2,3,4
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD
DWG NO.: <Doc>	Size C · Modify Date: Wednesday, December 18, 2013 · Sheet 7 of 25 · Rev 0


OUTPUT to VME CONNECTOR
U15C
EP3C40F780
LVDS Data To SLOT
SRAM LVDS ADDRESS
LVDS Data from SRAM
Spare LVDS I/O To/From S.B
FPGA
+2.5V BANK LVDS Interface
+2.5V BANK LVDS Interface
J7
16 pins IC Socket
U15D
EP3C40F780
SRAM INTERFACE (TTL)
SRAM Control
SLOT SPI
Single End Data to SRAM
Fast Monitoring Voltages
V,I Monitor ADC
FPGA
+3.3V BANK Single-End Interface
+3.3V BANK Single-End Interface
QuickUSB INTERFACE (TTL)
QuickUSB Control
QuickUSB DATA
QuickUSB ADDRESS
These Quick USB pins can be used for other function if not needed after done debugging
External ADC CMOS Level (L <0.3V, H > 1.4V)
DAC Control (L < 0.8V; H > 2.4V)
QuickUSB INTERFACE
Power Monitor ADC INTERFACE
FPGA SRAM INTERFACE
POWER SUPPLIES FAST MONITOR INTERFACE
WATCH FOR LIMITATION of NUMBER of OUPUT per BANK
1) LVDS receiver & emulated LVDS transmitter supported at all Banks
2) True LVDS transmitter supported at ONLY Banks 1,2,5,6
Bank 1,2,3,4,5,6 are for LVDS ONLY (Single end mix with LVDS will not be allowed by compiler)
PCB Mount low profile SMA
LOCAL CLOCK
7mm x 5mm S.M
I2C TEMPERATURE SENSOR
Agilent 16902B Logic Analyzer Connector (With 4 GHz timming plugin card 16910A) for MAIN FPGA (D0 to D15)
These LEDs are on Front Panel (RIGHT ANGLE through hole; 2/package; Dialight part number 552-0222F)
"MON_1_6_VOLTAGES_OK"
"Clock_OK"
"Slice_OK"
"Event_Out"
VME 3 rows- 96 pins back plane connector (This is NOT conform to VME signal standard)
LVDS Data TO Slots (1-8)
CLK & SLICE FROM Slot
CLK & SLICE TO Slot
To/From SLOT 1->8
These LED SHARES WITH LOGIC ANALYZER PINS
LBNL
Electronics Engineering Division
One Cyclotron Road
Berkeley, California 94720
Engineer: Chinh Vu
Designer: Judy Stirkkinen
DWG NO.: <Doc>
Title: FPGA Banks 5,6,7,8
Project: OPENPET- FAST DETECTOR BOARD
Modify Date: Wednesday, December 18, 2013
Sheet 8 of 25
Rev 0

When This light is "ON", USB connection is established



WARNING: Set Qusb_RESET_B = " LOW " could CRASH your PC

(Active Low reset OD input)
(48 MHz CPU Clock output)
(48 MHz GPIO Clock output)

Qusb Control lines

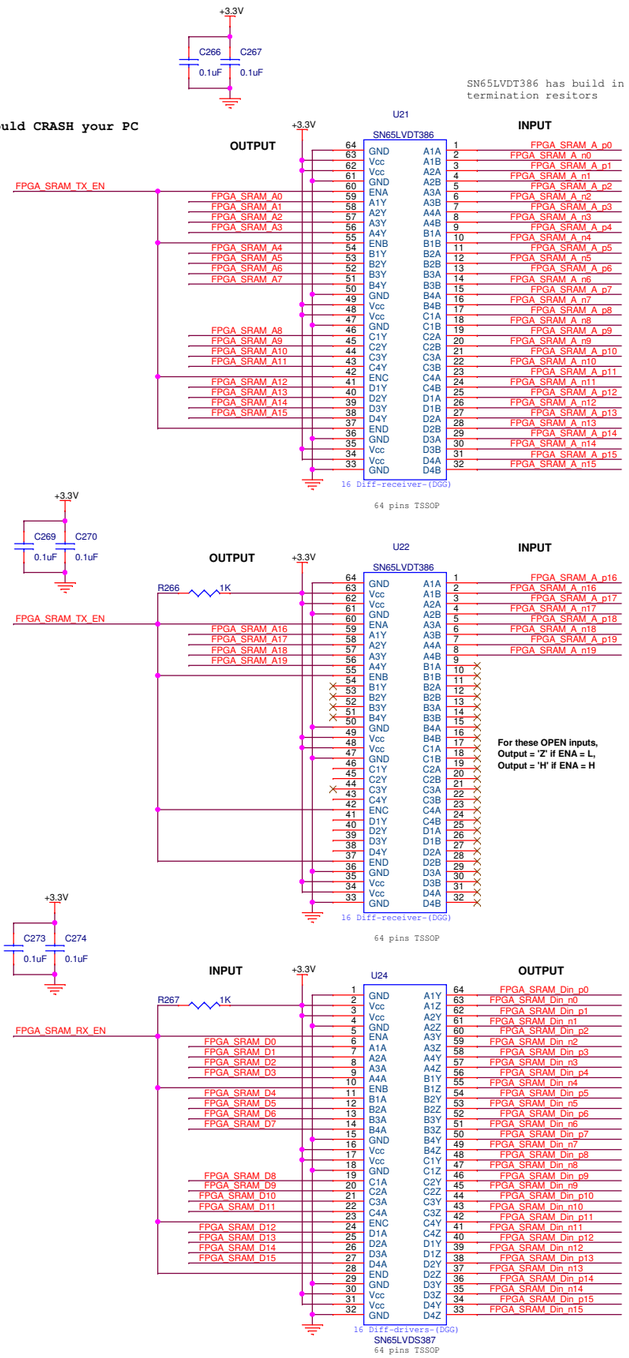
Qusb Control lines

Qusb ADR line

Optional circuit for independent debugging

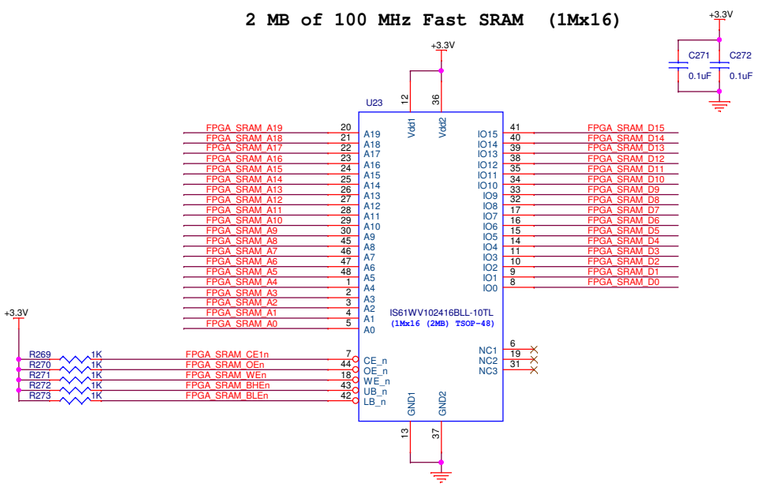
This is the 80 pins HIROSE S.M connector (1.25" x 0.25")

To the Host PC Interface plug-in Board VME connector



FPGA SRAM MEMORY

2 MB of 100 MHz Fast SRAM (1Mx16)



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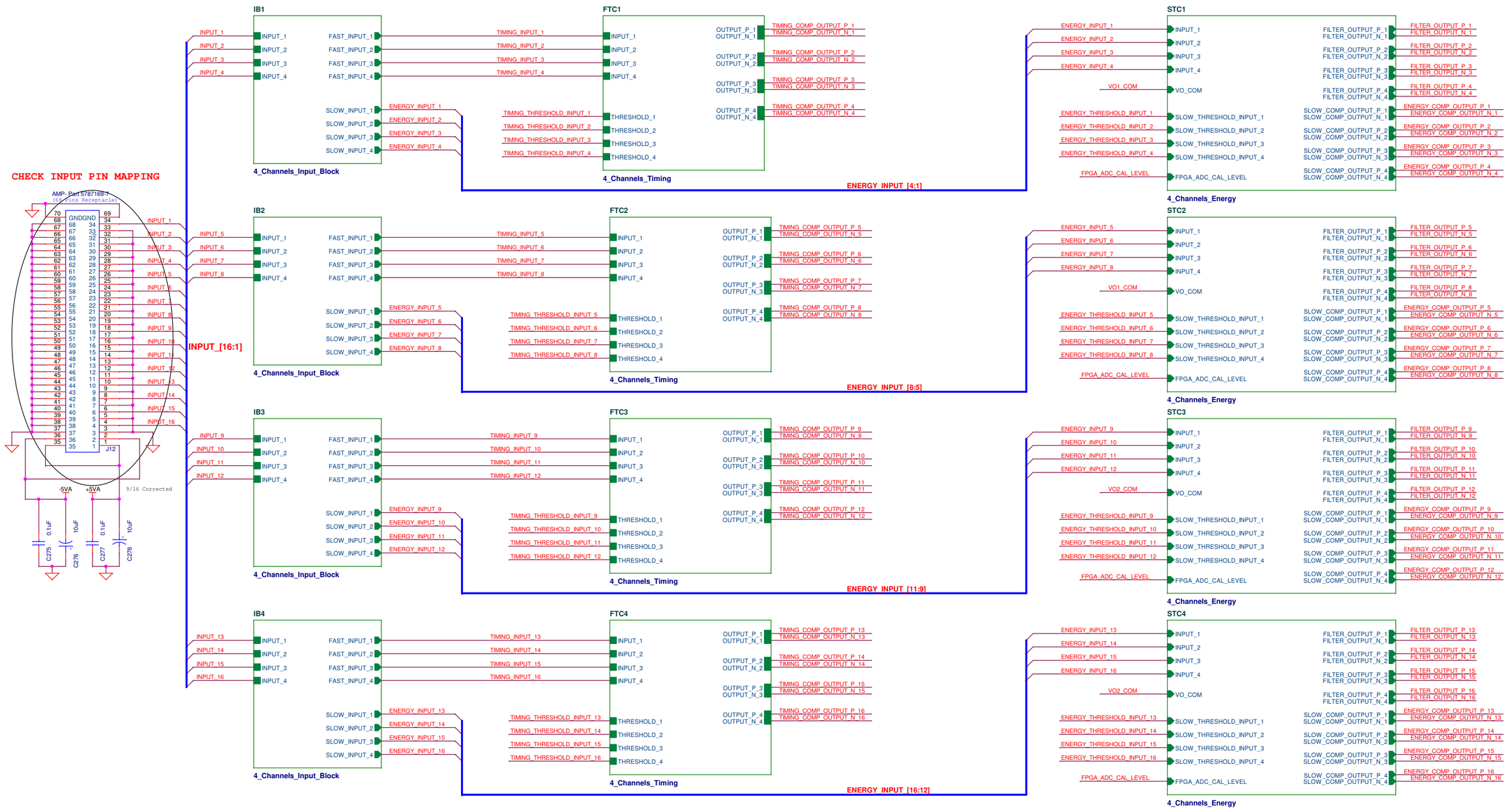
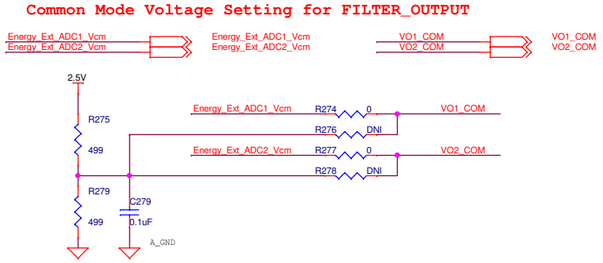
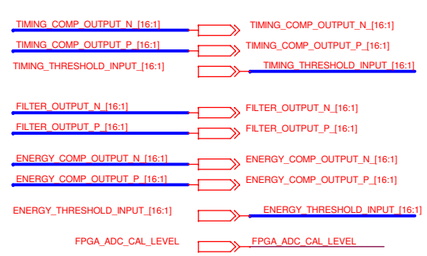
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL FA	
Engineer: Chinh Vu	Title: SRAM & Qusb Interface	
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD	
DWG NO.: <Doc>	Size D / Modify Date: Wednesday, December 18, 2013	Sheet 9 of 25 / Rev 0



Common Mode Voltage Setting for FILTER_OUTPUT





LAYOUT per group of 4 CHANNELS then duplicate 4 times

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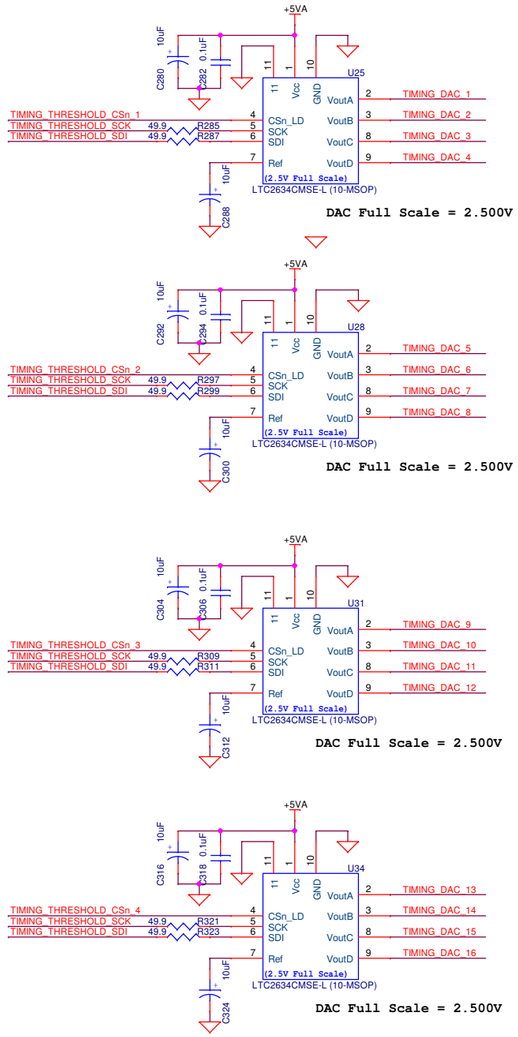
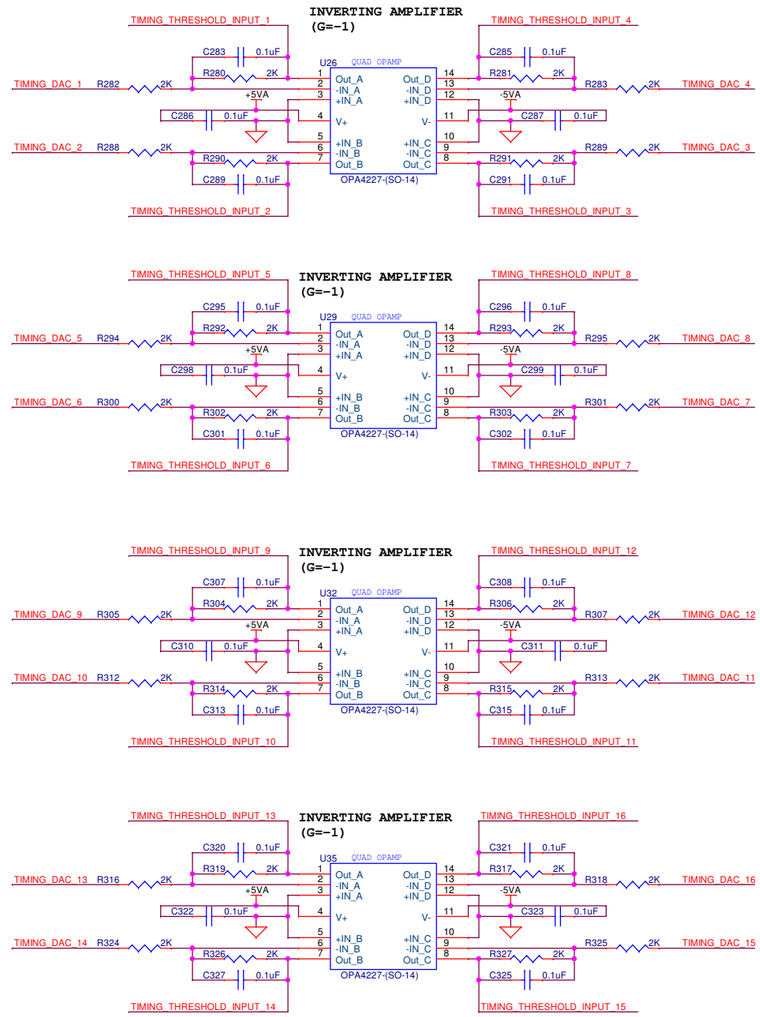
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL FA
Engineer: Chinh Vu	Title: FE 16 channels Analog Timing Chain TOP
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD
DWG NO.: <Doc>	Size C · Modify Date: Thursday, December 19, 2013 · Sheet 10 of 25 · Rev 0

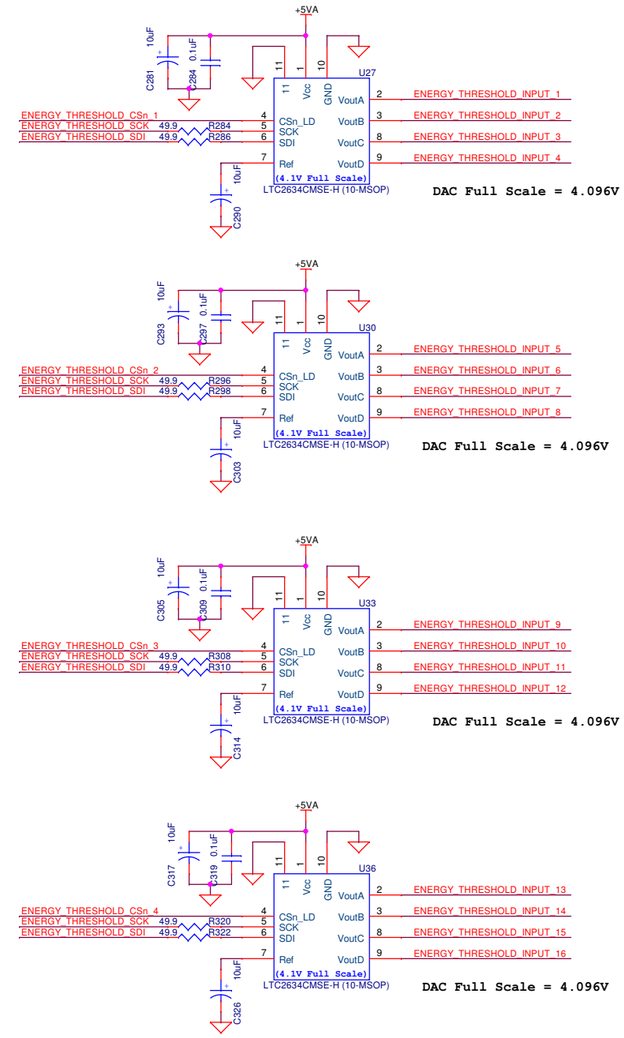
TIMING COMPARATOR THRESHOLD DAC



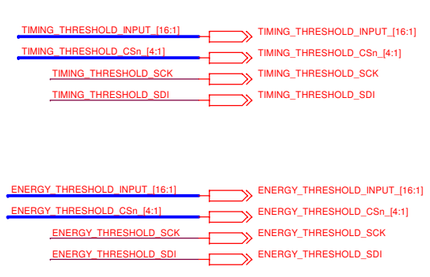
TIMING COMPARATOR THRESHOLD DAC INVERTER

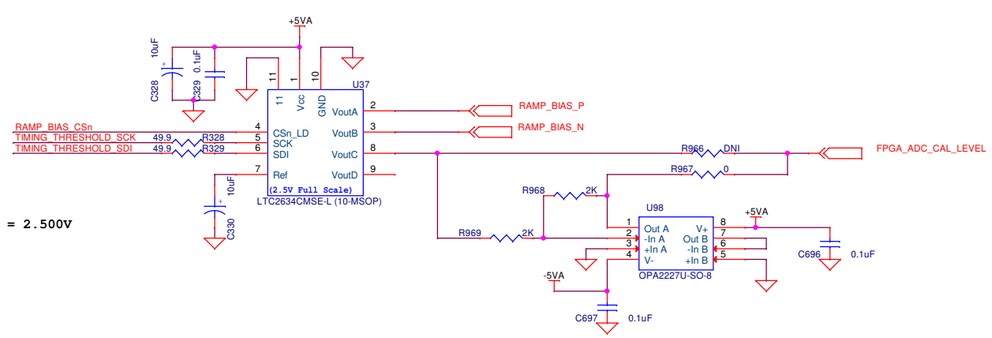


ENERGY COMPARATOR THRESHOLD DAC



LAYOUT EACH DAC OUPPUT WITH VIA TO ALLOW FOR PROBING





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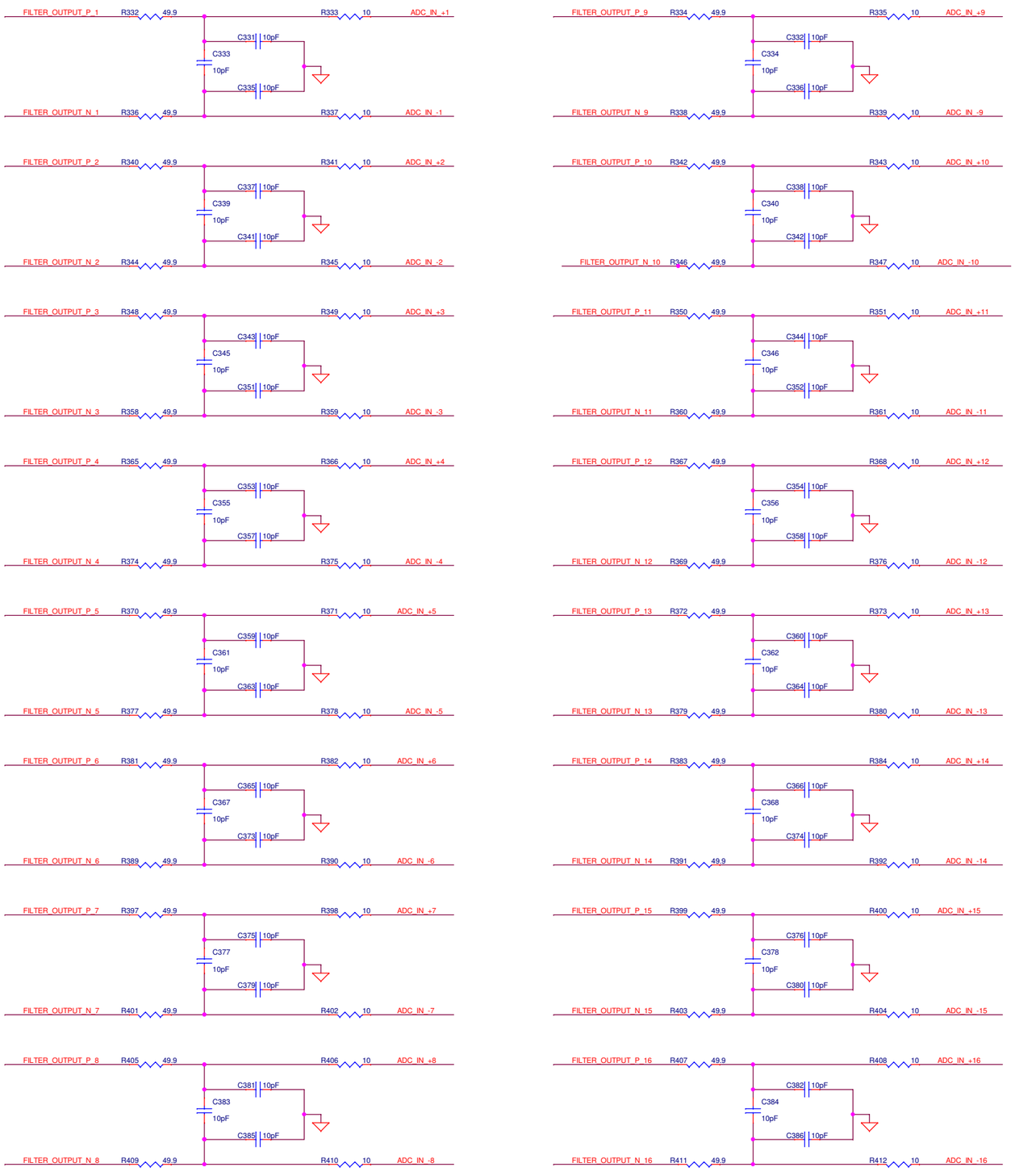
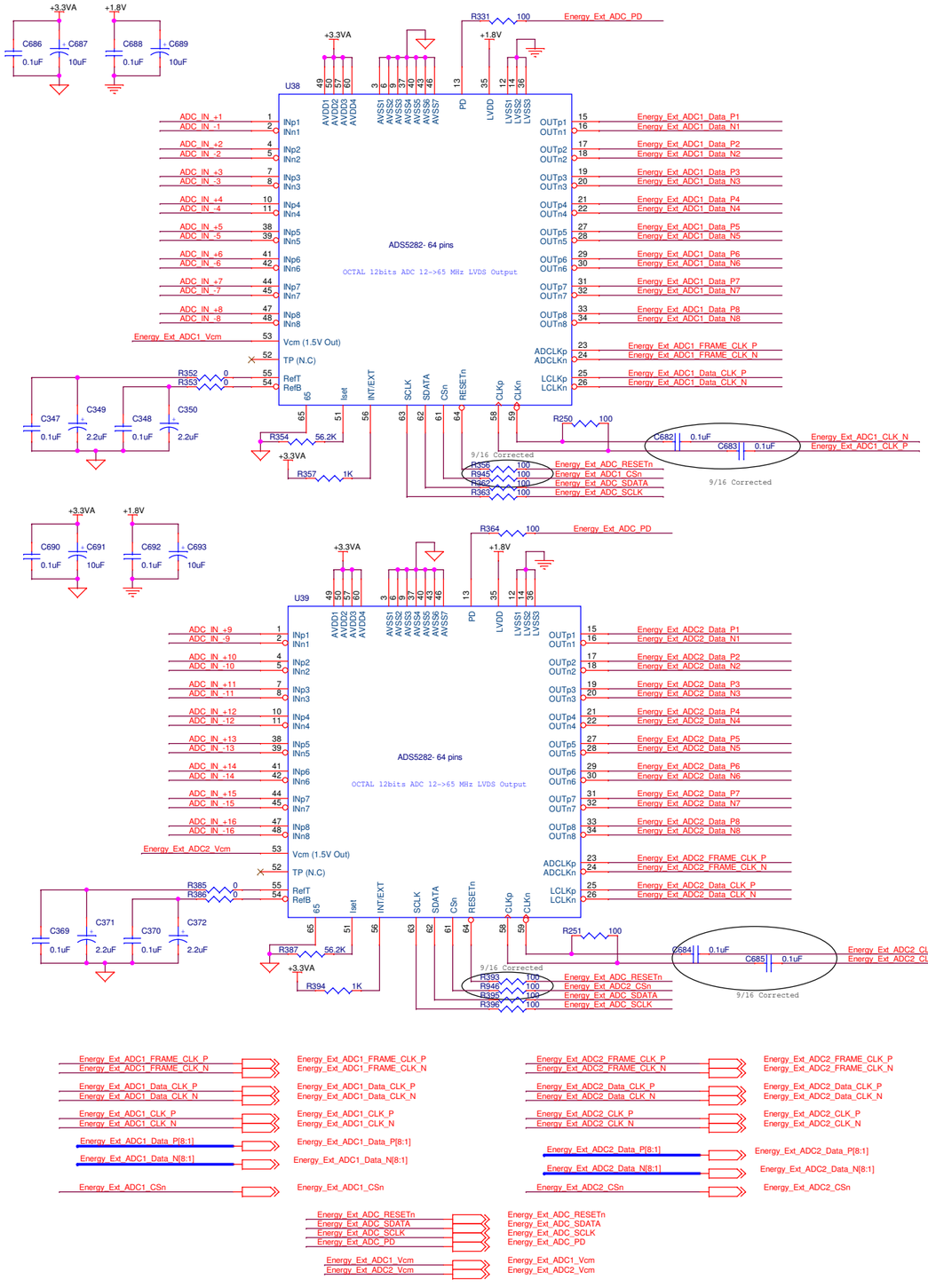
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD.16-CHANNEL FAST TIMIN
Engineer: Chinh Vu	Title: FE - DACs
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD
DWG NO.: <Doc>	Size C · Modify Date: Wednesday, December 18, 2013 · Sheet 11 of 25 · Rev 0





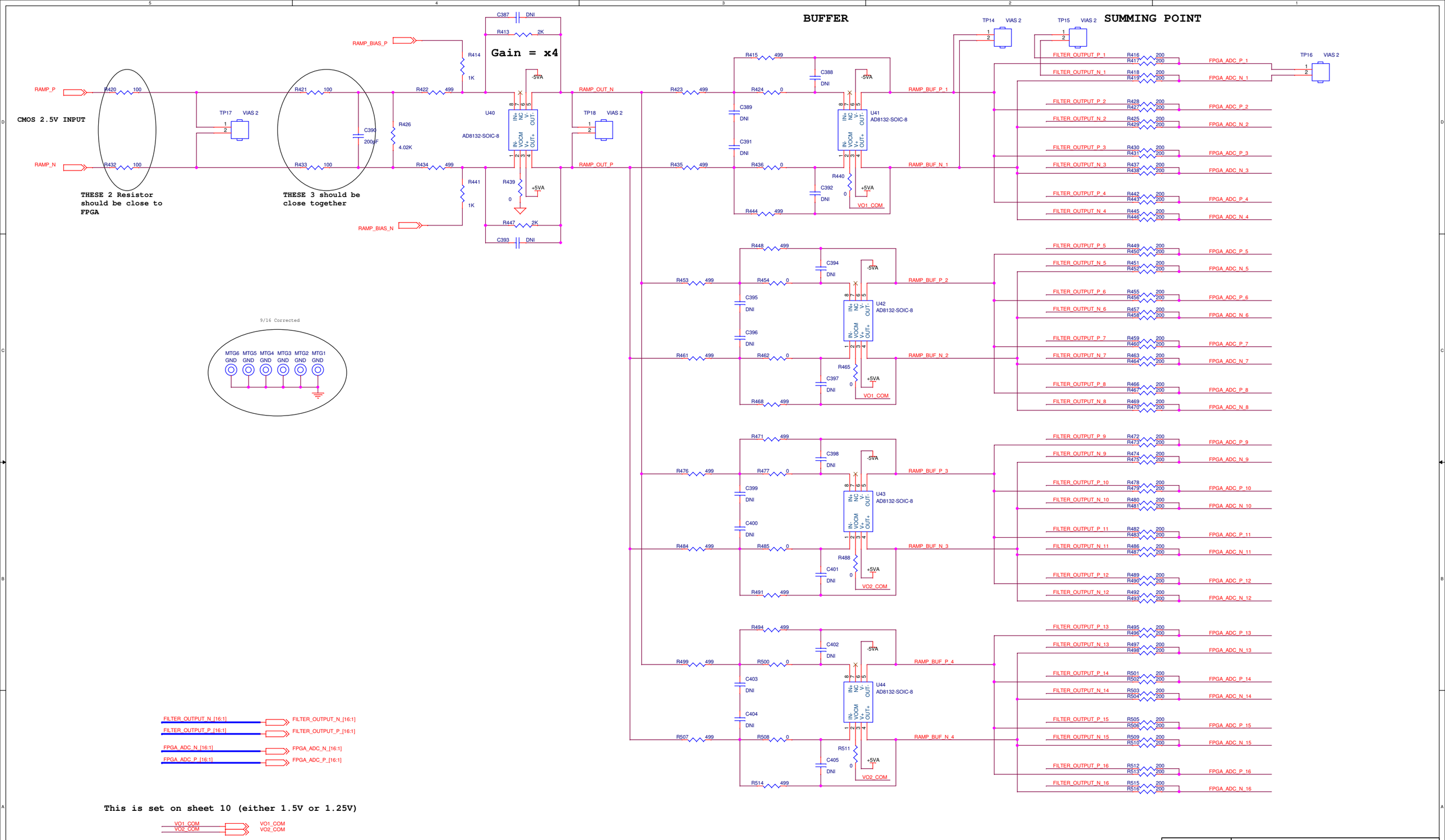
ADS5287 Notes:

1) AVDD = 3.3V; Vp-p = 2V; Vcom =1.5V; Cin-D=3pF
2) Digital are CMOS level

AD9212 ADC Notes:

1) AVDD = 1.8V; Vp-p = 2V; Vcom = AVDD/2; Cin-d =7pF

Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL FA
Engineer: Chinh Vu	Title: 16 Channels ADC
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD
DWG NO.: <Doc>	Size C · Modify Date: Wednesday, December 18, 2013 · Sheet 12 of 25 · Rev 0



Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720
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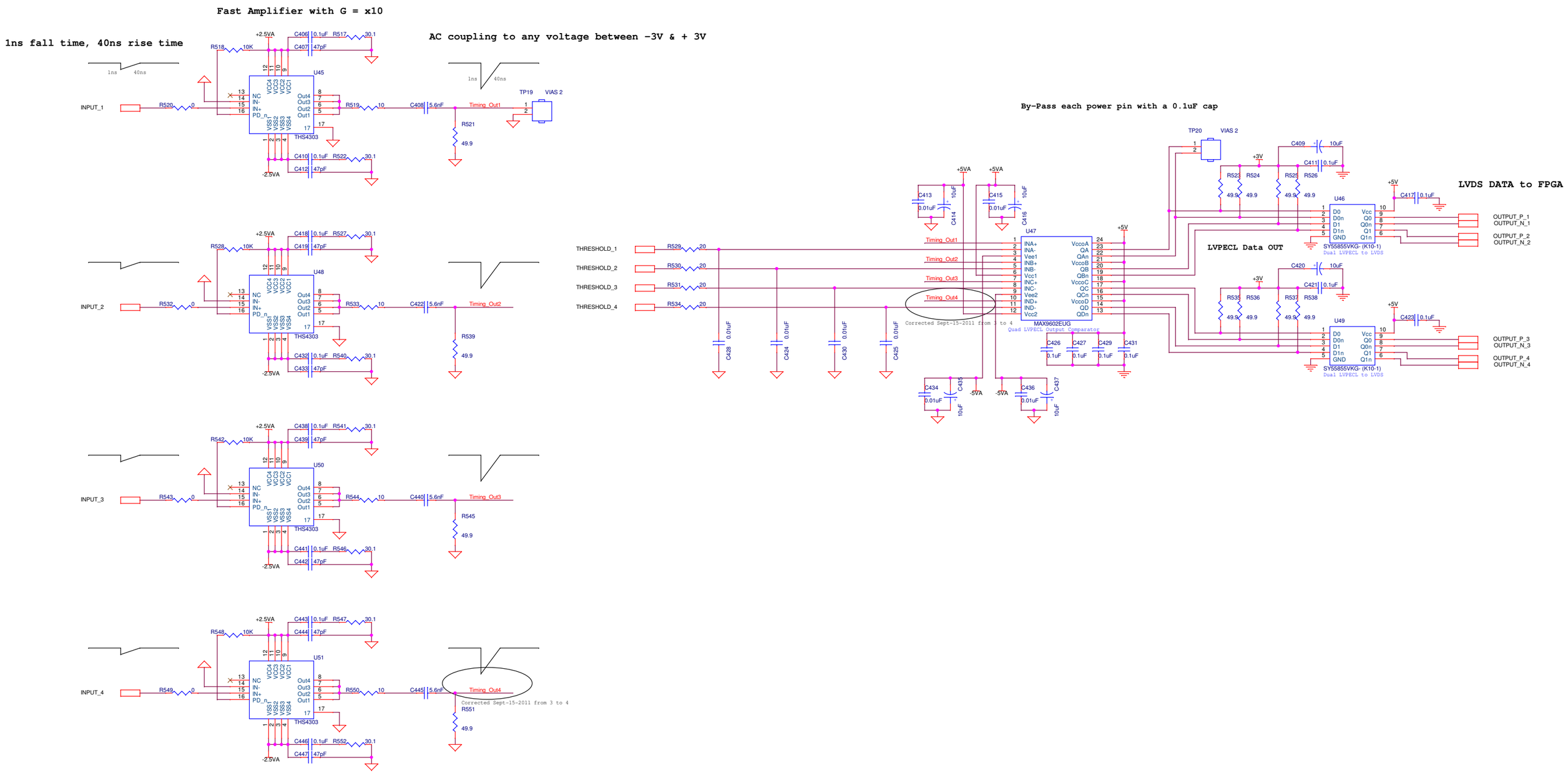
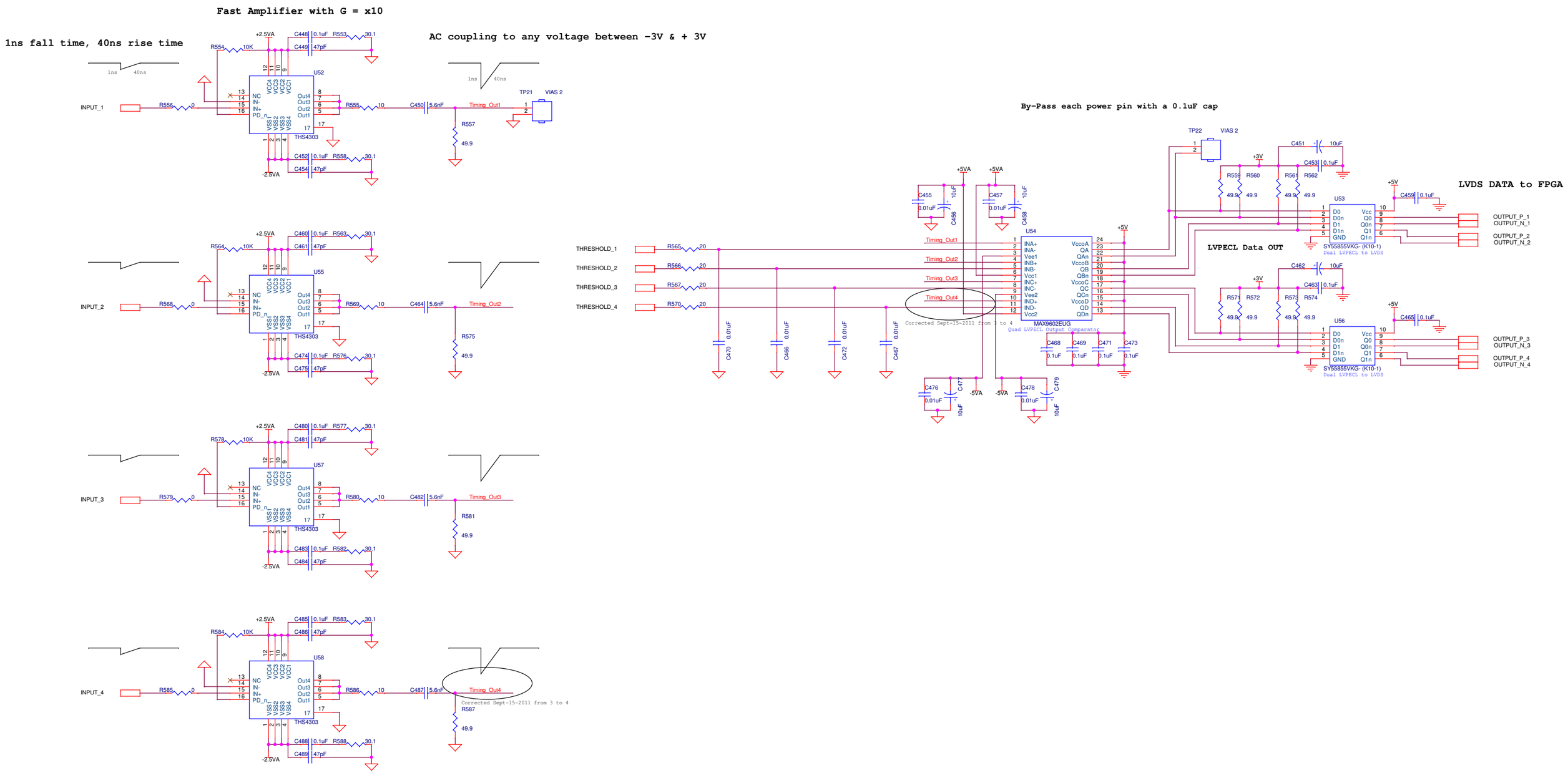
Engineer: Chinh Vu	Title: FPGA ADC RAMP
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD
DWG NO.: <Doc>	Size C · Modify Date: Wednesday, December 18, 2013 · Sheet 13 of 25 · Rev 0



Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL F
Engineer: Chinh Vu	Title: **4 CHANNELS FAST TIMING CHAIN**
Designer: Judy Stirkkinen	Project: **OPENPET- FAST DETECTOR BOARD**
DWG NO.: <Doc>	Size D · Modify Date: Wednesday, December 18, 2013 · Sheet 14 of 25 · Rev 0



Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL F
Engineer: Chinh Vu	Title: **4 CHANNELS FAST TIMING CHAIN**
Designer: Judy Stirkkinen	Project: **OPENPET- FAST DETECTOR BOARD**
DWG NO.: <Doc>	Size D · Modify Date: Wednesday, December 18, 2013 · Sheet 15 of 25 · Rev 0

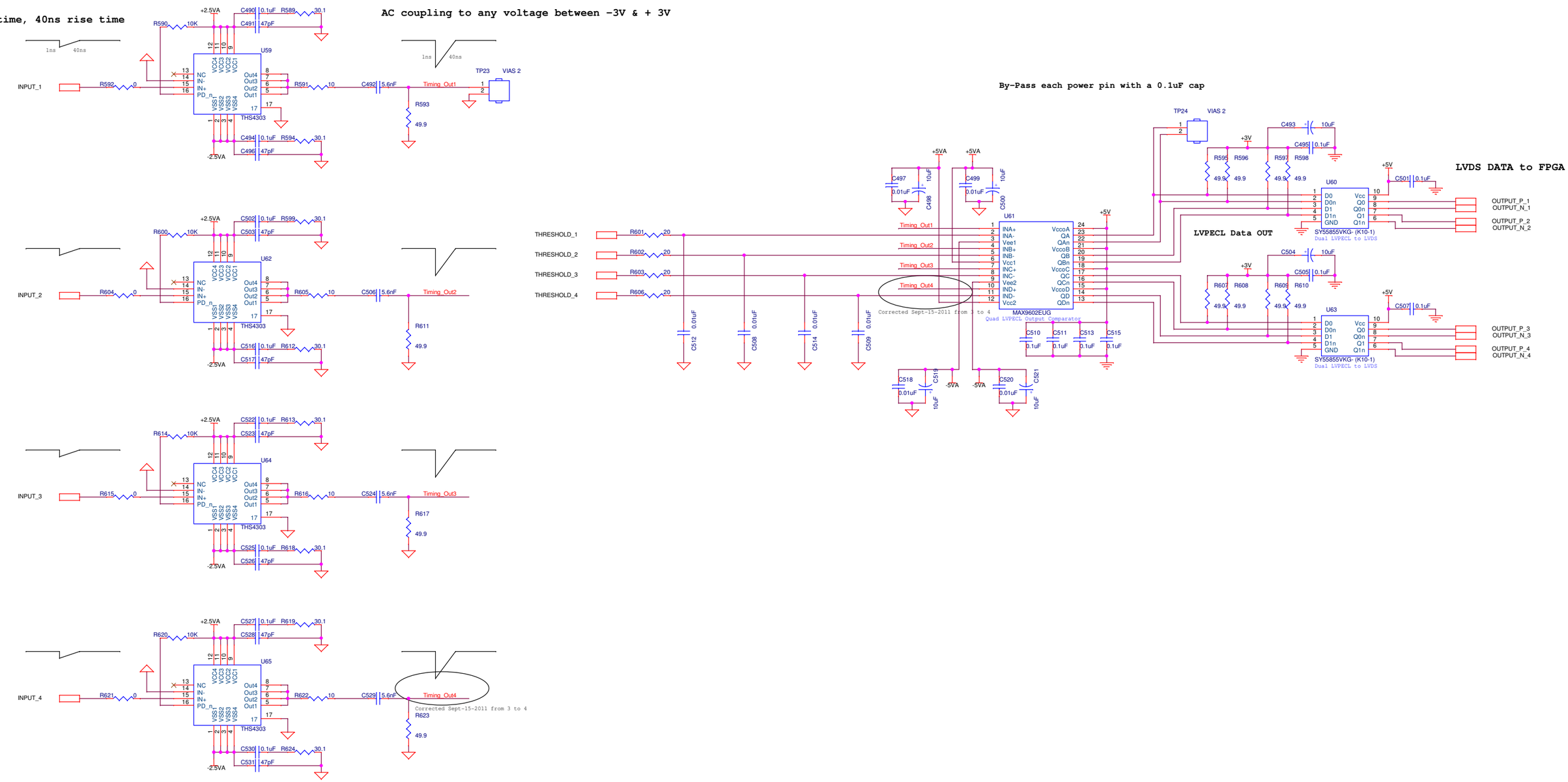
Fast Amplifier with G = x10

1ns fall time, 40ns rise time

AC coupling to any voltage between -3V & + 3V

By-Pass each power pin with a 0.1uF cap

LVDS DATA to FPGA



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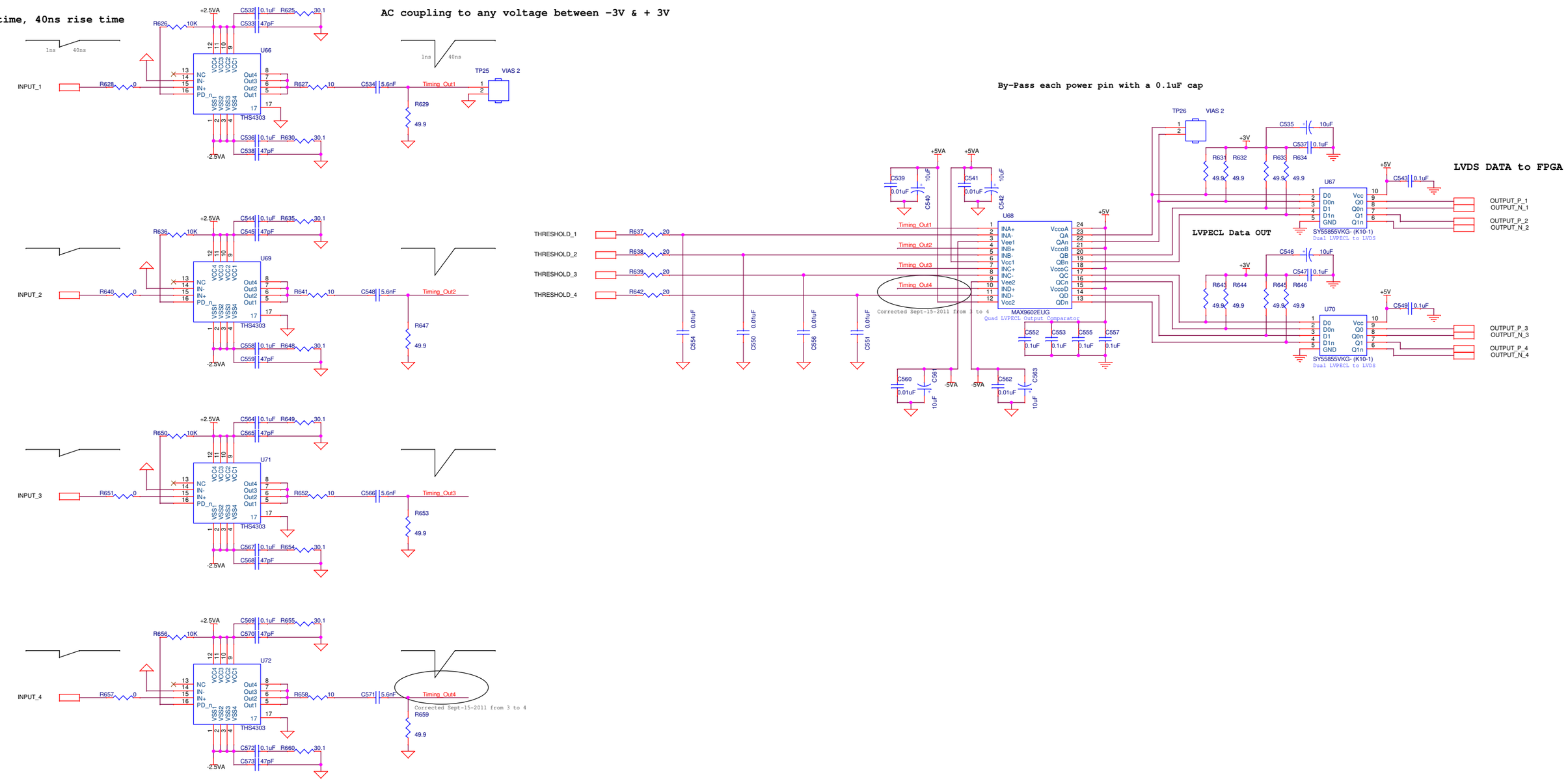
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL F
Engineer: Chinh Vu	Title: **4 CHANNELS FAST TIMING CHAIN**
Designer: Judy Stirkkinen	Project: **OPENPET- FAST DETECTOR BOARD**
DWG NO.: <Doc>	Size D · Modify Date: Wednesday, December 18, 2013 · Sheet 16 of 25 · Rev 0

Fast Amplifier with G = x10

1ns fall time, 40ns rise time

AC coupling to any voltage between -3V & + 3V

By-Pass each power pin with a 0.1uF cap



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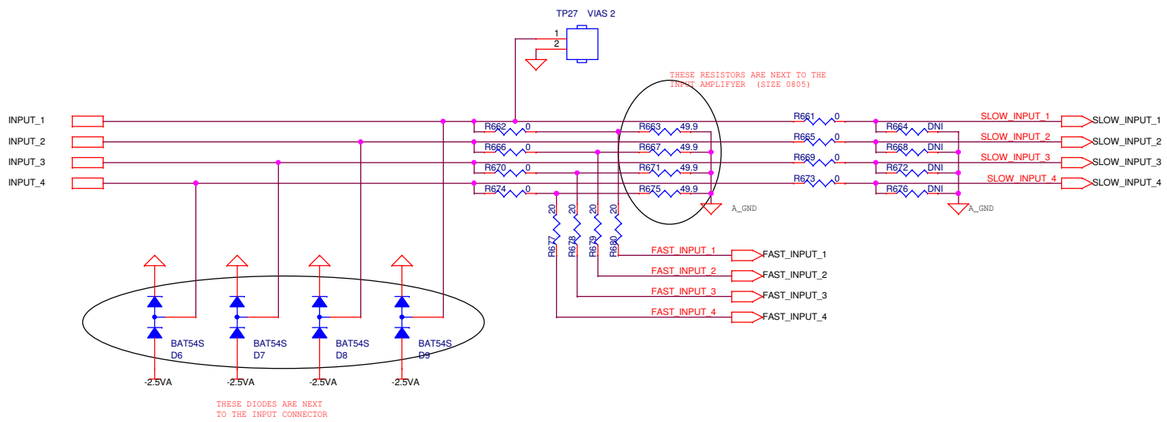
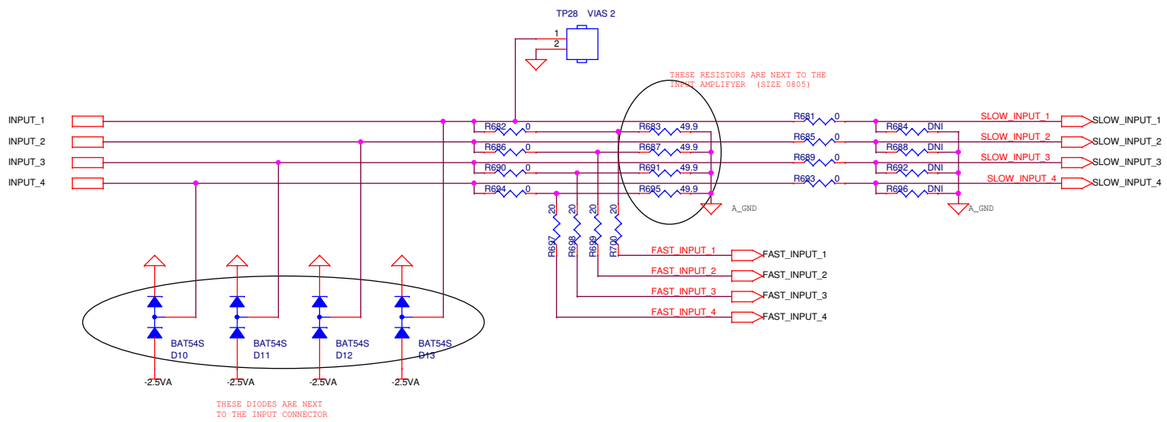
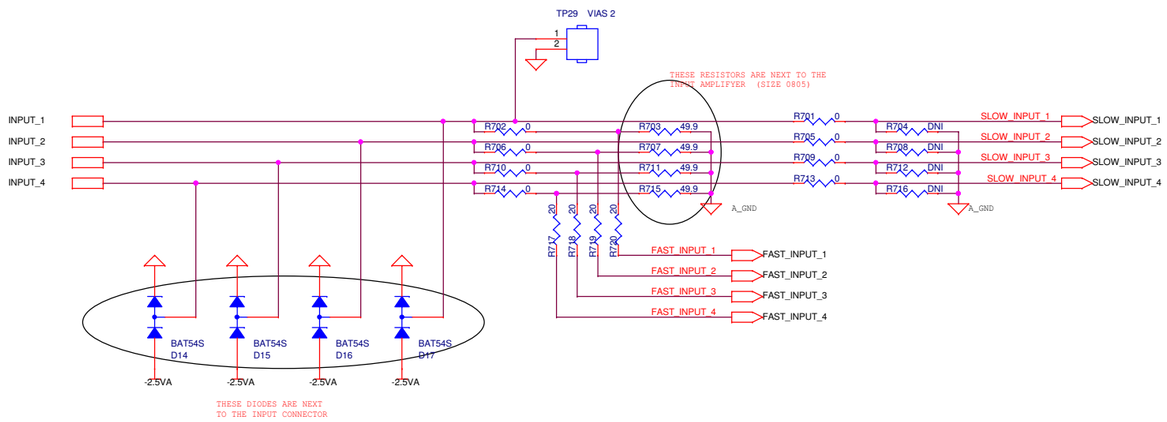
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL F
Engineer: Chinh Vu	Title: **4 CHANNELS FAST TIMING CHAIN**
Designer: Judy Stirkkinen	Project: **OPENPET- FAST DETECTOR BOARD**
DWG NO.: <Doc>	Size D · Modify Date: Wednesday, December 18, 2013 · Sheet 17 of 25 · Rev 0



Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL FA	
Engineer: Chinh Vu	Title: 4 CHANNELS INPUT RESISTORs	
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD	
DWG NO.: <Doc>	Size C / Modify Date: Wednesday, December 18, 2013	Sheet 18 of 25 / Rev 0



Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720	
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL PA	
Engineer: Chinh Vu	Title: 4 CHANNELS INPUT RESISTORs	
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD	
DWG NO.: <Doc>	Size C / Modify Date: Wednesday, December 18, 2013	Sheet 19 of 25 / Rev 0



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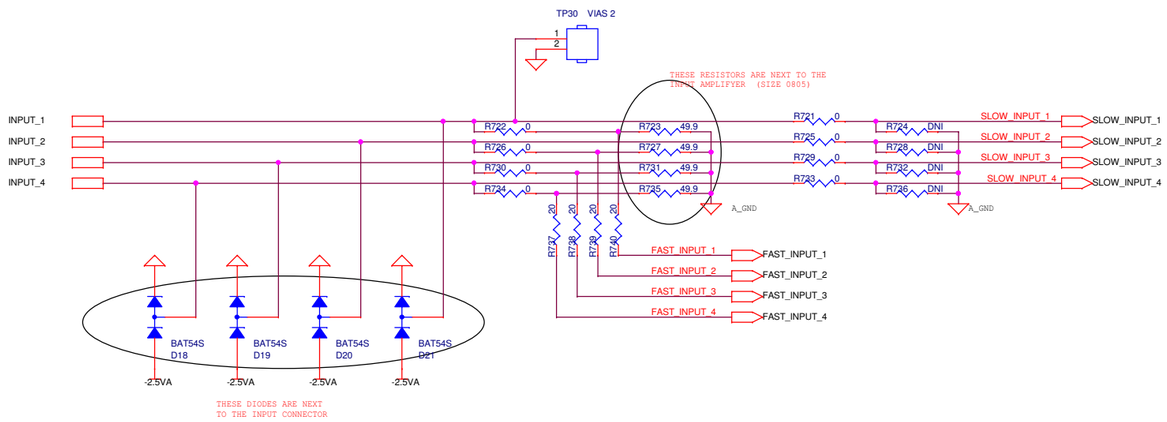
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL FA	
Engineer: Chinh Vu	Title: 4 CHANNELS INPUT RESISTORs	
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD	
DWG NO.: <Doc>	Size C — Modify Date: Wednesday, December 18, 2013	Sheet 20 of 25 — Rev 0



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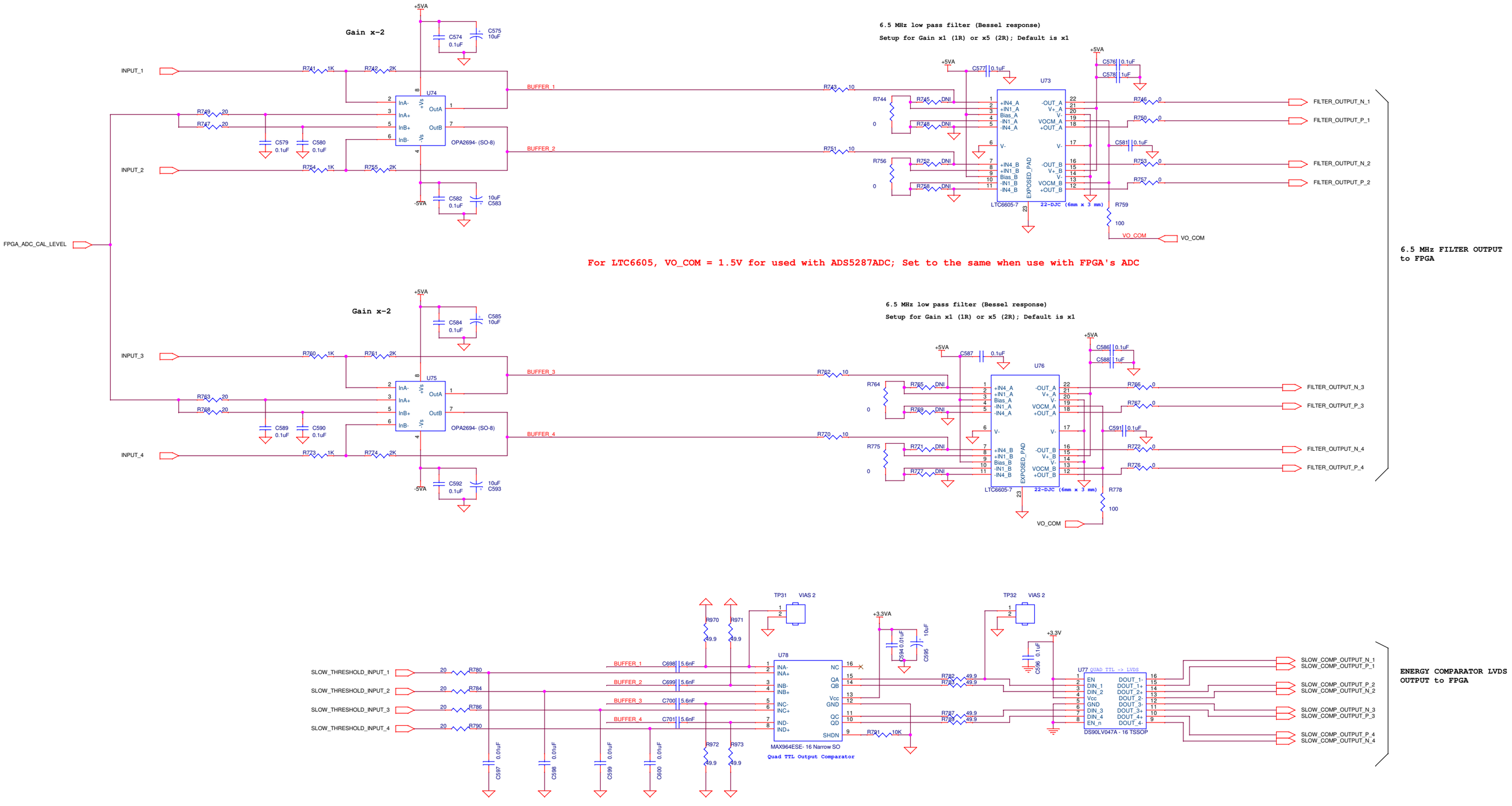
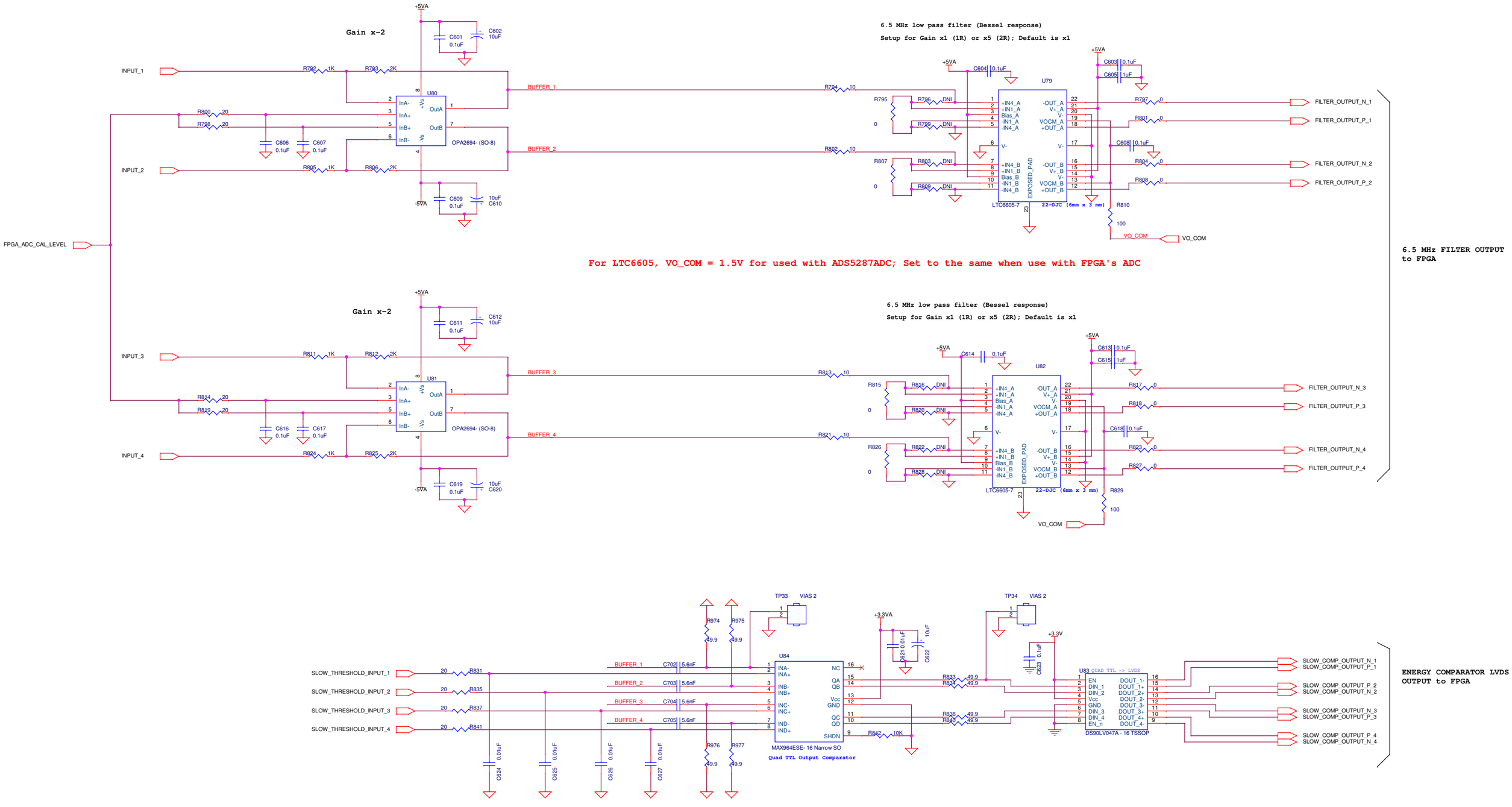
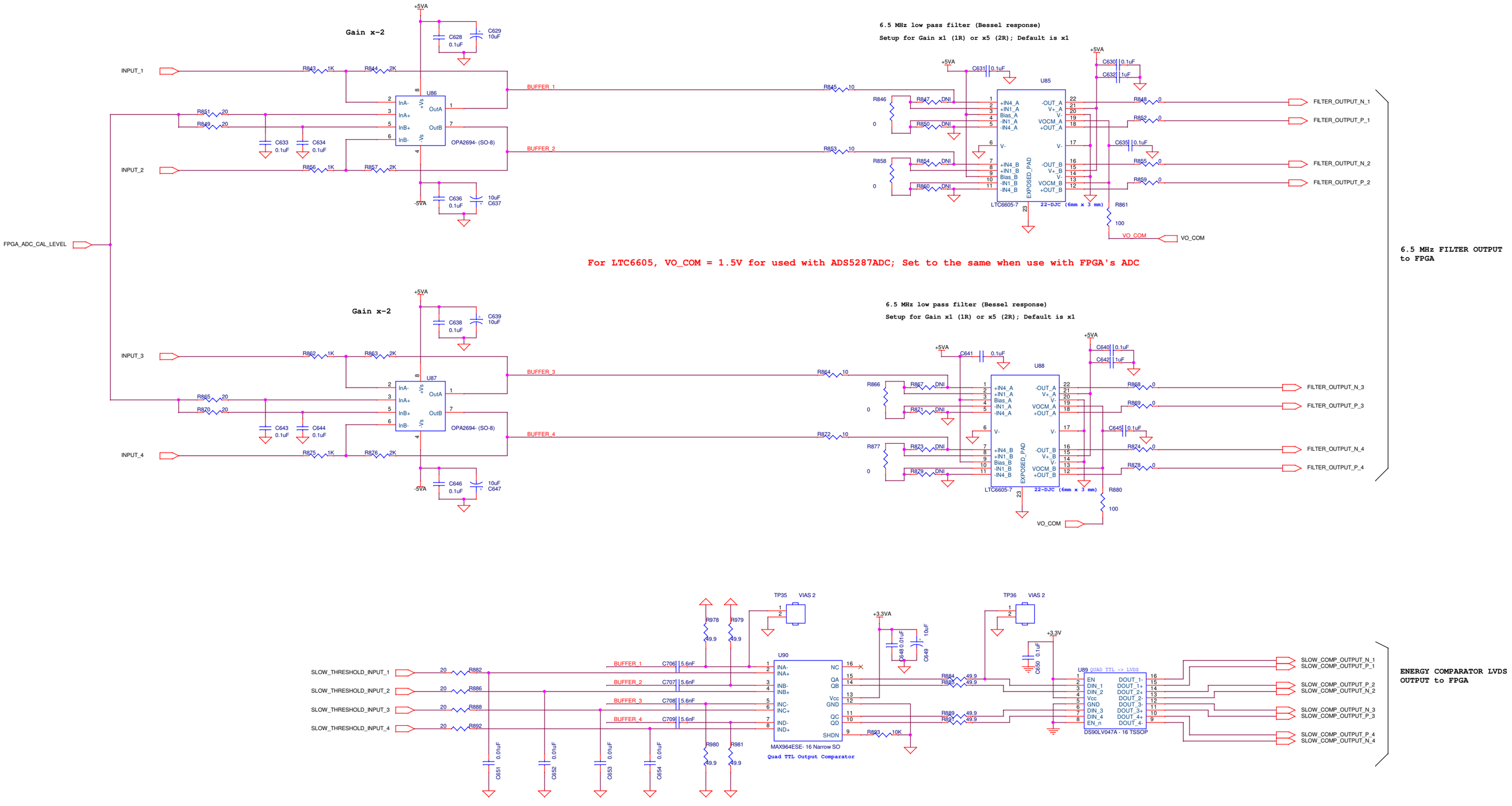
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL FA	
Engineer: Chinh Vu	Title: 4 CHANNELS INPUT RESISTORs	
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD	
DWG NO.: <Doc>	Size C / Modify Date: Wednesday, December 18, 2013	Sheet 21 of 25 / Rev 0



Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL PA
Engineer: Chinh Vu	Title: 4 CHANNELS SLOW TIMING CHAIN
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD
DWG NO.: <Doc>	Size C · Modify Date: Wednesday, December 18, 2013 · Sheet 22 of 25 · Rev 0



Revisions:	LBNL Electronics Engineering Division One Cyclotron Road Berkeley, California 94720
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL F/
Engineer: Chinh Vu	Title: 4 CHANNELS SLOW TIMING CHAIN
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD
DWG NO.: <Doc>	Size C · Modify Date: Wednesday, December 18, 2013 · Sheet 23 of 25 · Rev 0



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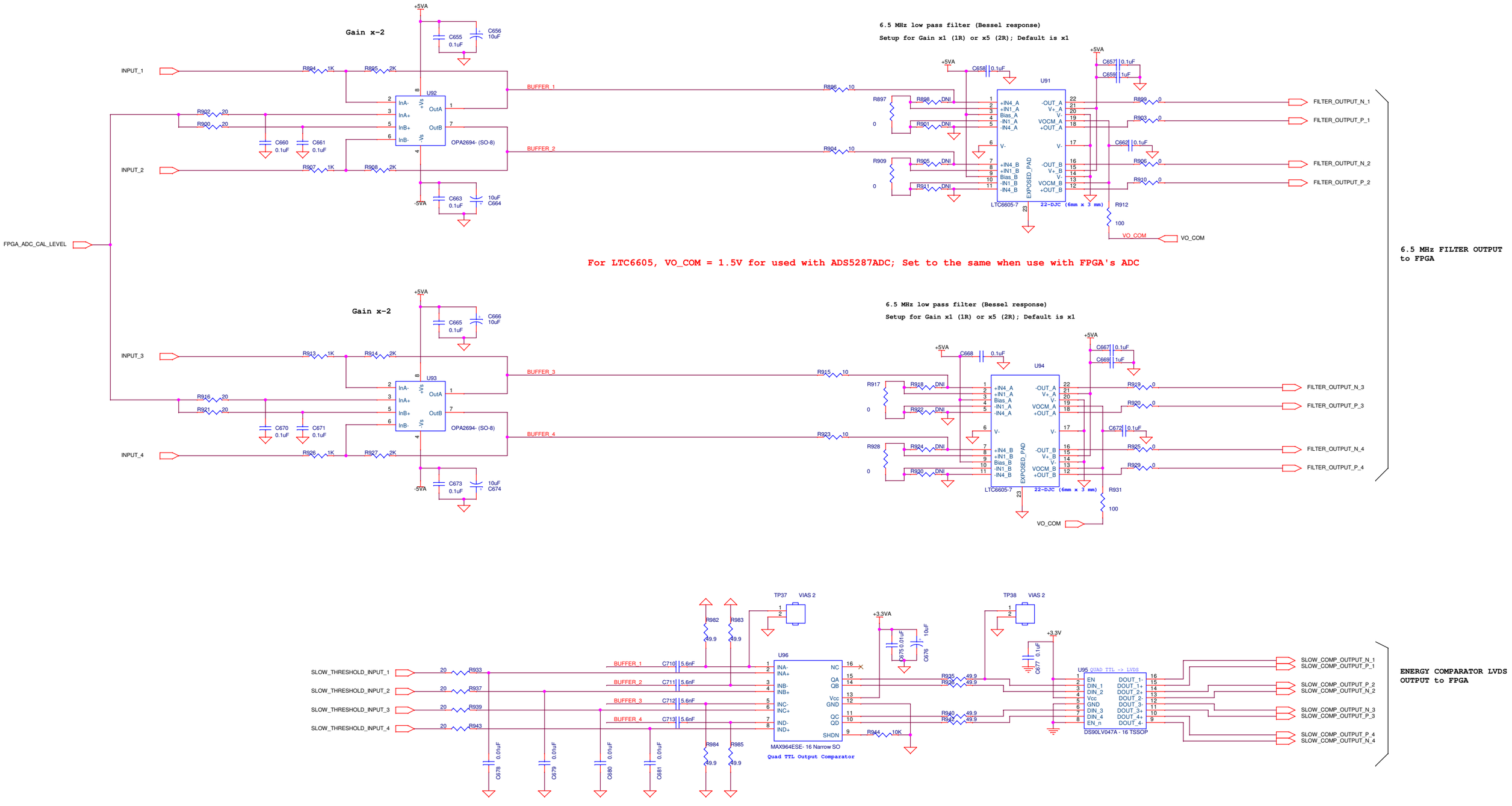
	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL PA
Engineer: Chinh Vu	Title: 4 CHANNELS SLOW TIMING CHAIN
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD
DWG NO.: <Doc>	Size C · Modify Date: Wednesday, December 18, 2013 · Sheet 24 of 25 · Rev 0



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	C:\USERS\SENG\DOCUMENTS\ORCAD\OPENPET\DETECTOR BOARD\16-CHANNEL F/
Engineer: Chinh Vu	Title: 4 CHANNELS SLOW TIMING CHAIN
Designer: Judy Stirkkinen	Project: OPENPET- FAST DETECTOR BOARD
DWG NO.: <Doc>	Size C · Modify Date: Wednesday, December 18, 2013 · Sheet 25 of 25 · Rev 0