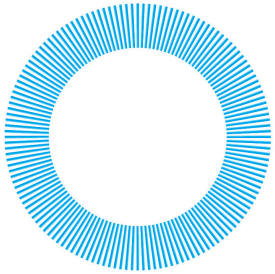

openPET

A Flexible Electronics System for Radiotracer Imaging

Introduction & Overview	*Bill Moses*
Detector Board	*Carl Jackson*
Support / Coincidence Board	*Seng Choong*
Programming Tools / Environment	*Qiyu Peng*
Schedule	*Carl Jackson*

November 4, 2010

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openPET Vision

General-Purpose Electronics & Software for Nuclear Medical Imaging Cameras

Open Source

- Hardware, Firmware, and Software
- Schematics, Gerbers, BOM,…

Active User Community

- Share Software and Expertise
- Module, Calibration, DAQ, Display,…

http://OpenPET.LBL.gov

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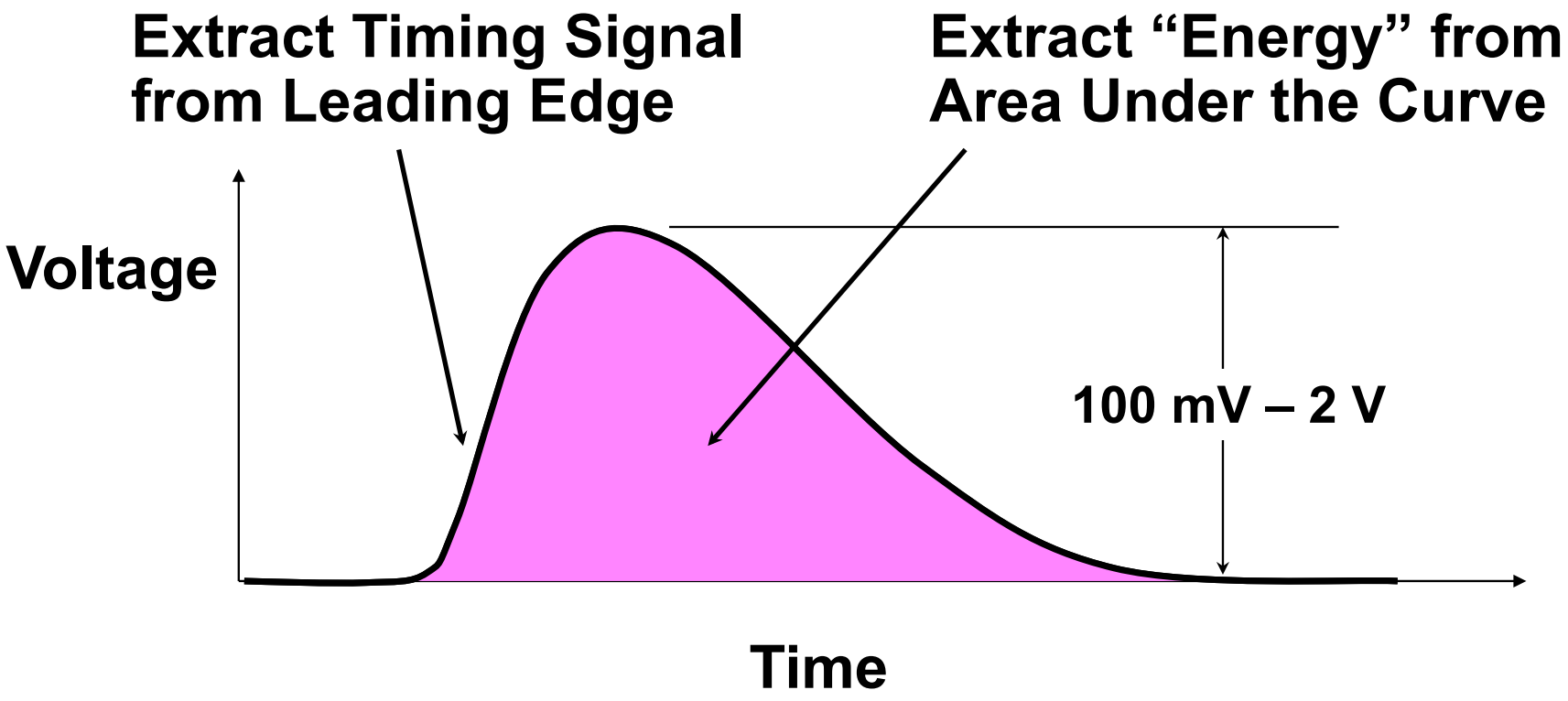
All Detector Outputs Look the Same



- *Tremendous* Variation in How Outputs Are Combined
  ⇒Combine Outputs in Firmware

Electronics System Requirements

High-Performance

- # of Channels, Rate, Energy, Timing, …

***Very* Flexible**

- Type of Detector, Camera Configuration, Event Word Definition

User-Modifiable

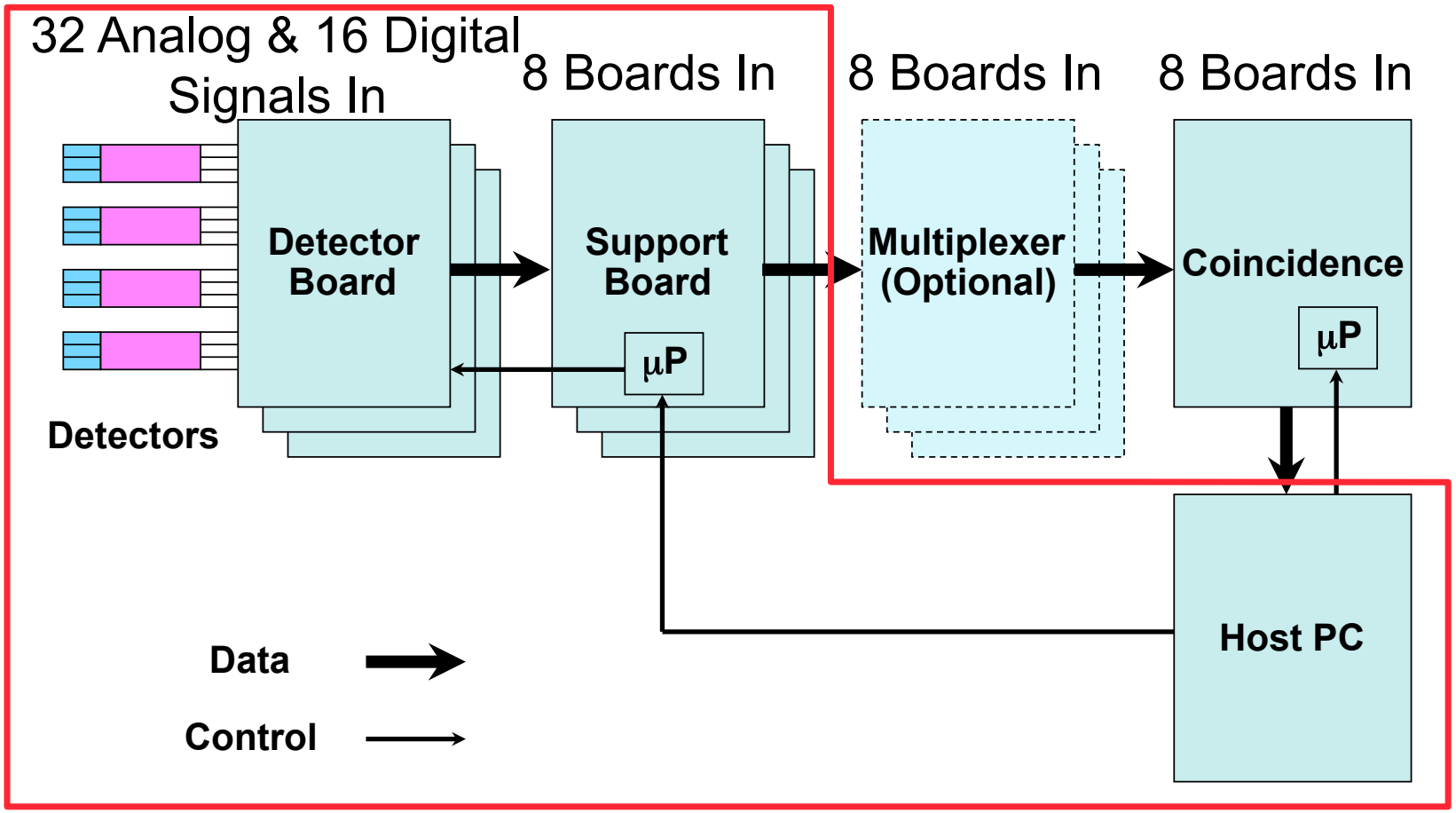
- Schematics, Source Code, Knowledge Base

User-Friendly

- Instructions, Documentation, Can Buy Boards

Like Open Source Software

OpenPET System Architecture



- Supports 512 Block Detectors (4096 With Multiplexers)
- PSB + 8 DPBs Makes Nice Test Stand (64 Block Detectors)

Changes in the Last Year

Detector Board

- 16→32 Channels per Board
- 16 Differential Digital IO Lines per Board

Support Board

- More Interface Options (RS-232)
- More Memory (2 GB)

Coincidence Board

- Now Same Hardware as Support Board (programmed with different FPGA equations)

Most in Response to User Suggestions—Thanks!!!

Form Factor Defined

Same as 12-Slot VME 6-U Crate

- Connectors in Different Locations
  - Avoid accidently plugging in VME boards!
- 8 Input Slots
  - Detector Boards if acting as Support Board
  - Support Boards if acting as Coincidence Board
- 4 Slots for “Plug-In” Boards
  - Interface to Host PC
  - Interface to Coincidence Board
  - User IO
  - Debugging

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Tidbits…

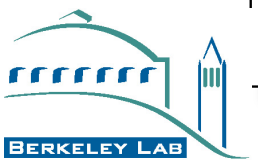
Web Site Recently Updated

- New Version of Specification
- Another Version Expected Soon
- Copies of Publications & Presentations

Seeking Collaborator for Software Librarianship

- Organize Software & Firmware
- Moderate Modifications, Additions, and Variants

http://OpenPET.LBL.gov



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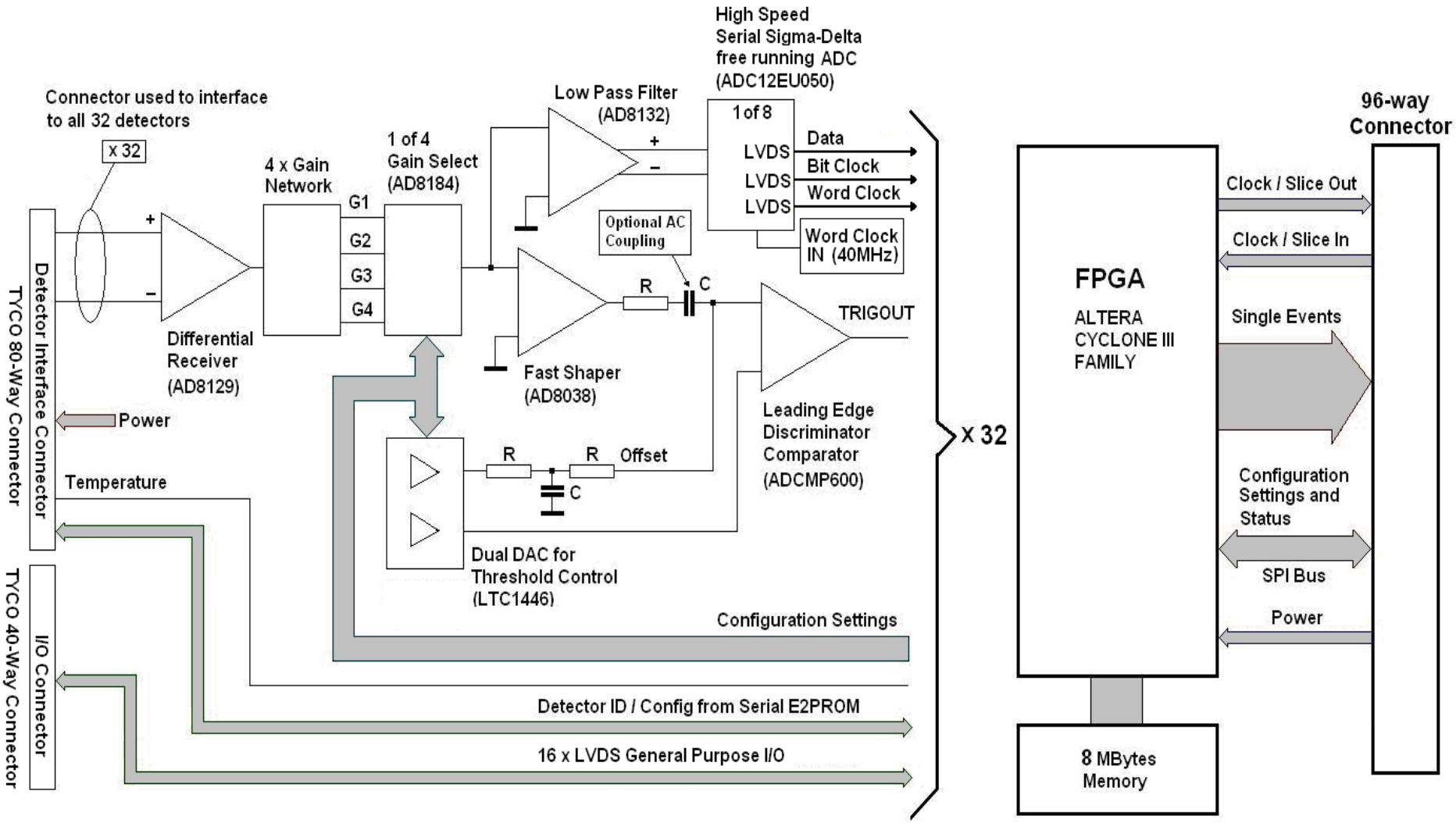
Detector Support Board



DSB Key Features

Connections

- DSB is VME ‘B-size’ with 96-way connector for interfacing to OpenPET bus

- Front panel has 2 connectors:

  80-way for analog inputs from detectors, power, low-speed digital communication, and bias voltage (±100V)

  40 way for 16 user definable LVDS digital I/O ports

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Analog Inputs

- 32 Differential analog inputs from detectors (PMT, SPM etc)
- Each input has fast shaper for event detection and TDC time-stamping
- Each input has fast free-running ADC readout for energy measurement

NOTE:

The 32 analog lines can be configured for 32 individual detector inputs or up to 16x16 cross-wire matrix readout

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FPGA functions

- FPGA implements TDC (at present 0.5ns). Can be improved to < 100ps
- FPGA responsible for configuration of DACs etc via commands from backplane
- FPGA responsible for detecting events and reporting position, energy + TDC value
- FPGA passes single event data to OpenPET backplane
- 8 MBytes of memory available. FPGA can use for ROI lookup tables etc.

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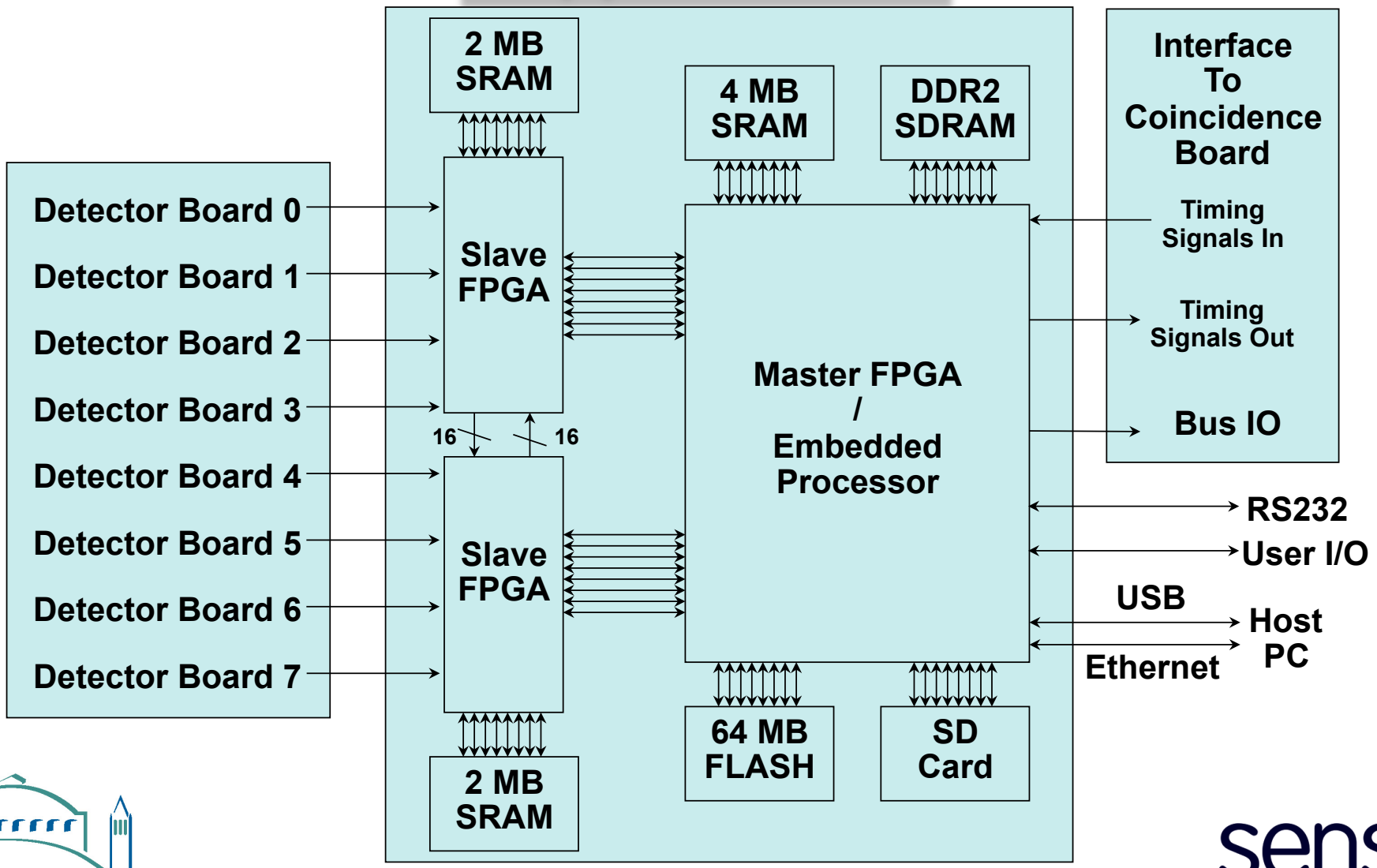
Support Board



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Plug-In Boards

1. **Host PC Interface**

   The front panel of this board would have an Ethernet connector, USB connector, SD card connector, reset switch, and a few basic LEDs

2. **Coincidence Board Interface**

   The front panel of this board would have a connector that would attach to a cable that goes to the coincidence board.

3. **User I/O**

   The front panel would have connectors for two RS-232 cables, an External Clock input, and 32 External Digital IO lines.

4. **Debugging**

   The front panel would have a JTAG connector, two connectors for logic analyzers, and lots of LEDs.

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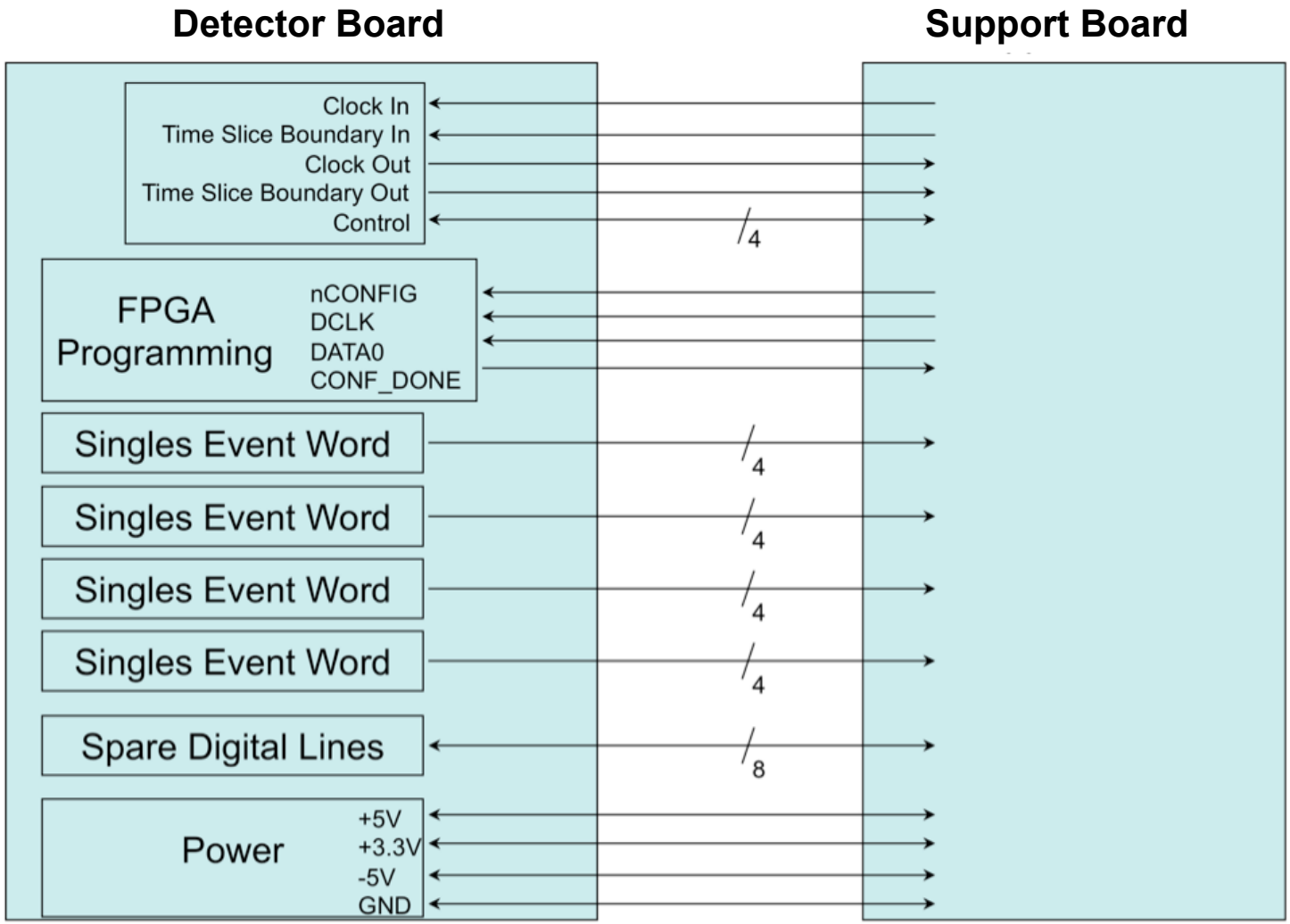
Detector Board to Support Board Bus IO



Connector Between Detector Board and Support Board

	A	B	C
1	D0+	GND	D1+
2	D0-	3.3V	D1-
3	D2+	GND	D3+
4	D2-	+5V	D3-
5	D4+	GND	D5+
6	D4-	-5V	D5-
7	D6+	GND	D7+
8	D6-	3.3V	D7-
9	D8+	GND	D9+
10	D8-	+5V	D9-
11	D10+	GND	D11+
12	D10-	-5V	D11-
13	D12+	GND	D13+
14	D12-	3.3V	D13-
15	D14+	GND	D15+
16	D14-	+5V	D15-
17	GND	-5V	GND
18	CLK_IN+	3.3V	CLK_OUT+
19	CLK_IN-	+5V	CLK_OUT-
20	GND	-5V	GND
21	SLICE_IN+	3.3V	SLICE_OUT+
22	SLICE_IN-	GND	SLICE_OUT-
23	GND	NC	GND
24	SPARE0+	SPARE1+	SPARE2+
25	SPARE0-	SPARE1-	SPARE2-
26	SPARE3+	SPARE4+	SPARE5+
27	SPARE3-	SPARE4-	SPARE5-
28	SPARE6+	SPARE7+	CTRL_CS
29	SPARE6-	SPARE7-	CTRL_CLK
30	CTRL_DO	NC	CTRL_DI
31	DCLK	DETECTOR BIAS	DATA0
32	nCONFIG	3.3V	CONF_DONE

Color	Group Description
	LVDS Data to DB FPGA & Coincidence Board
	Clock & Slice IN/OUT
	Undefined pins between DB FPGA & DSB FPGA
	Slow control SPI interface signals
	DB FPGA serial programming pins
	No connection
	Power & GND
	Detector Bias Voltage (100 V max.)

Connector is
96 pin VME Connector

On DB
Vector Electronics RE96MSR-062
(Digi-Key part # V1235-ND)

On PB
Vector Electronics RE96FSP
(Digi-Key part # V1240-ND)

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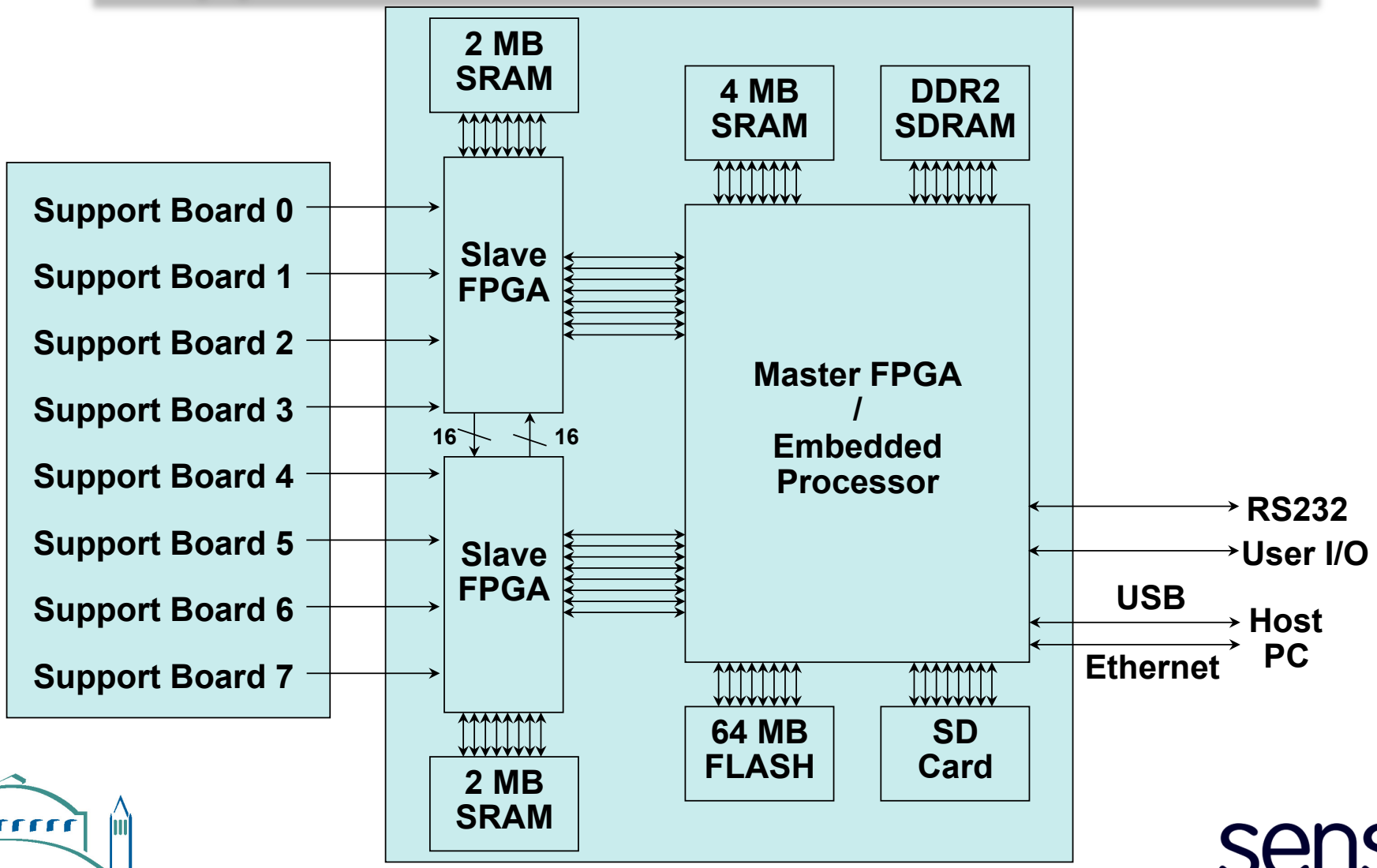
Support Board As Coincidence Board



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Programming Tools / Environment

Qiyu Peng

Firmware and Software Requirements

	Detector Board	Support Board	Coincidence Board	Host PC
FPGA Firmware	X	X	X	
Embedded Microprocessor Software		X	X	
PC Software				X

X: Altera free design tools

X: NI LabWindows/CVI ($2,599)

- **Hardware requirements:**

✓ PC

✓ Altera USB-blaster download cable (for downloading and debugging)

Tasks of FPGA Firmware

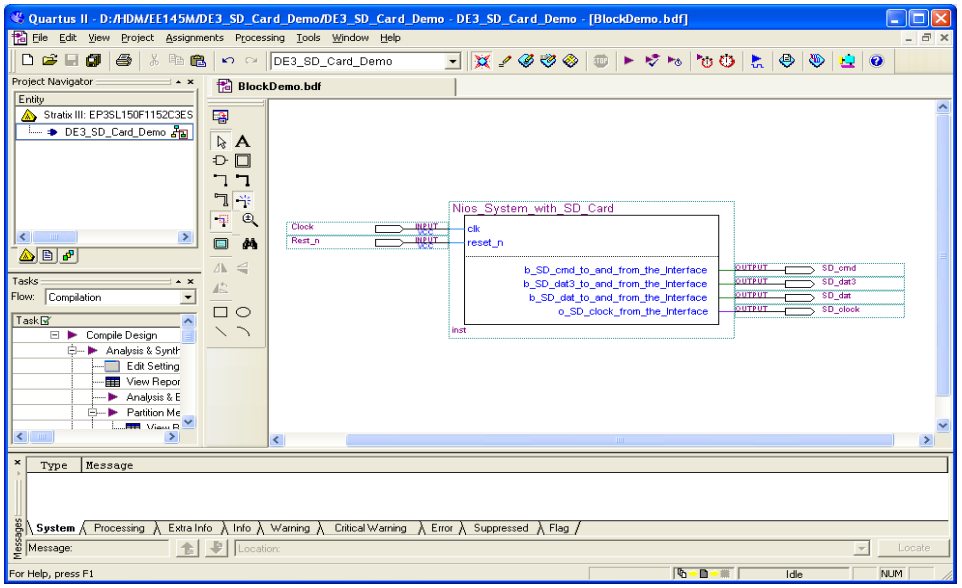
- **Detector Board**
  - Read out ADCs
  - Read out TDCs
  - Combine ADC and/or TDC information to form single event words
- **Support Board**
  - Multiplex Single event words to coincidence board
  - Configure, control and test detector board
- **Coincidence Board**
  - Identify coincident signals
  - Format coincidence words
  - Send data to Host PC

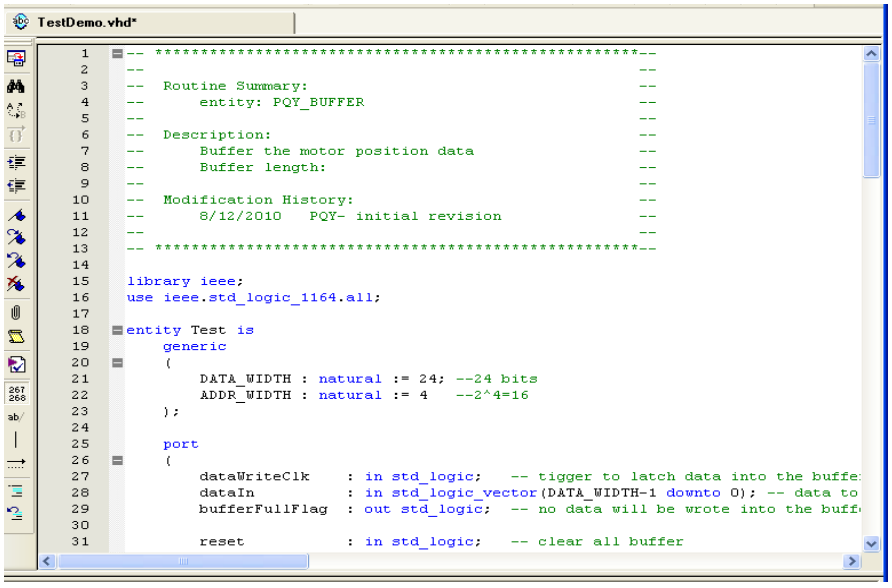
Functionalities of Software

- **Support Board (Nios II Embedded Microprocessor)**
  - Configure, test, calibrate, and monitor detector board
  - Test, control and monitor support board
- **Coincidence Board (Nios II Embedded Microprocessor)**
  - Configure, control and monitor detector board
  - Multiplex single event words to coincidence board
- **Host PC**
  - High level control, configuration, calibration and monitor of all the boards
  - Receive data flow from the coincidence board

FPGA Firmware

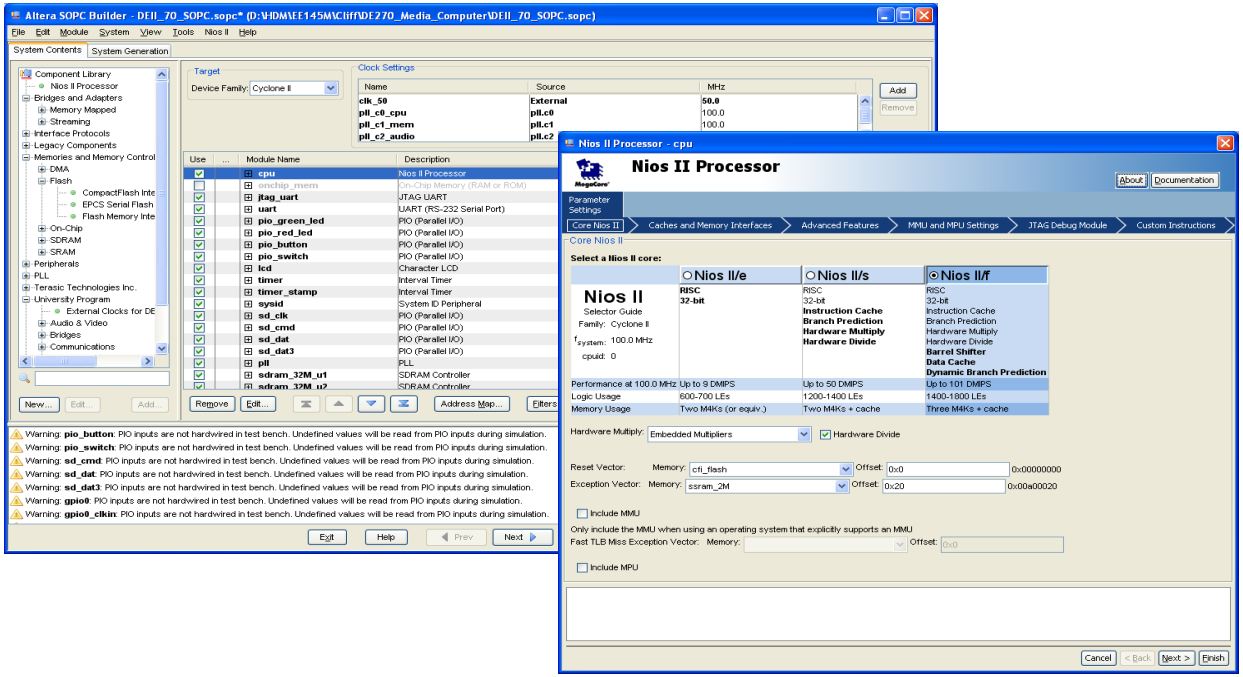
- **Design Software: Quartus II Web Edition 10.0 (Free)**
  https://www.altera.com/download/software/quartus-ii-we
- **Design Language: Schematic and VHDL**





Embedded Microprocessor Software

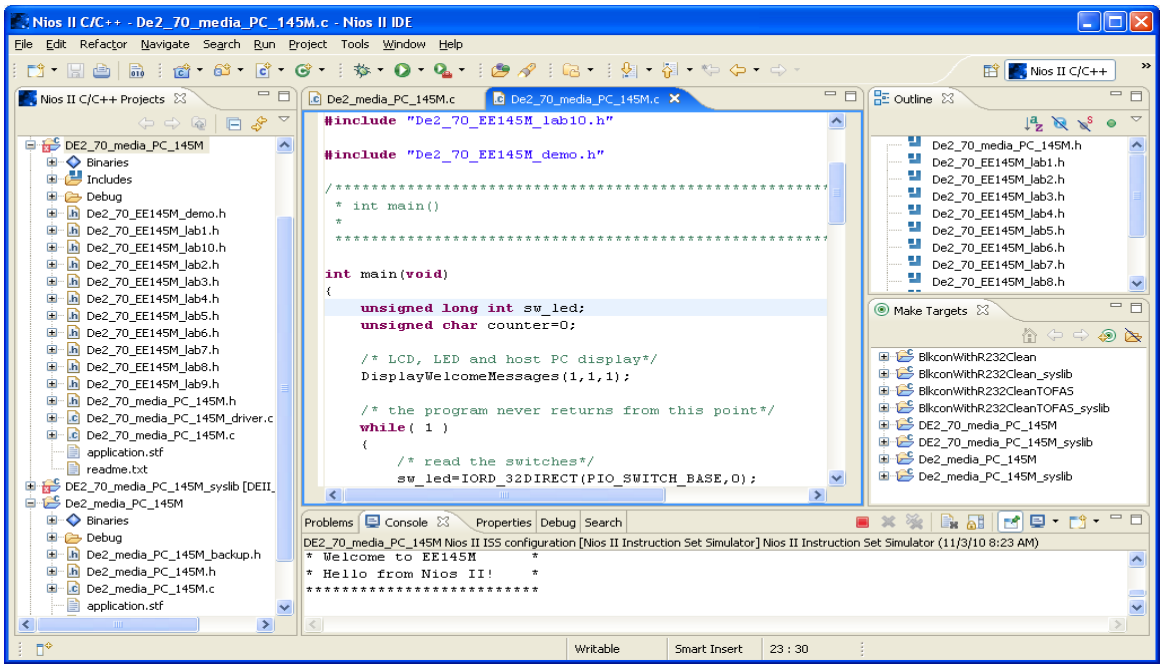
- **CPU Design Software: SOPC, comes with Quartus II Web Edition 10.0 (Free)**
- **Design Language: N/A**



We will design the µ-processor. You shouldn't need to modify it.

Embedded Processor Software

- **Design Software: Altera Nios II Embedded Design Suite v10.0 (Free)**
  https://www.altera.com/download/service-packs/sps-nios-ii.jsp#10.0-sp1
- **Design Language: Standard C**

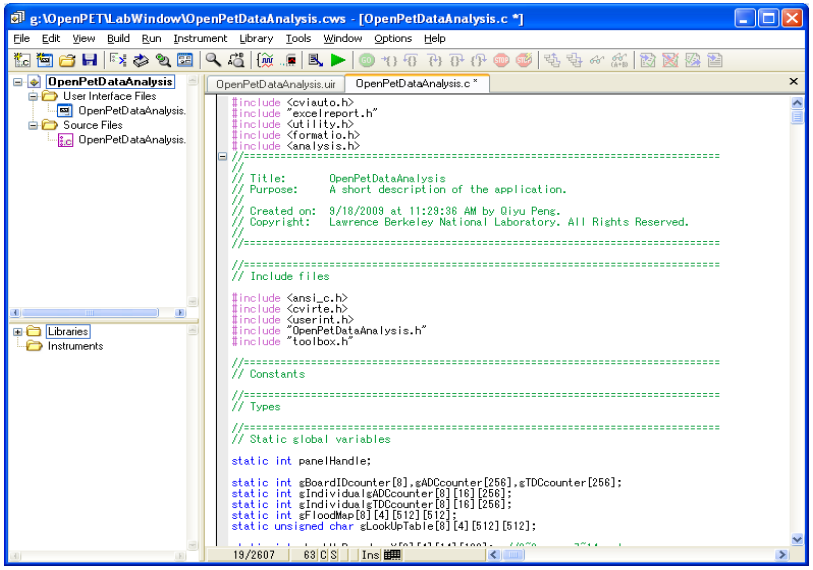


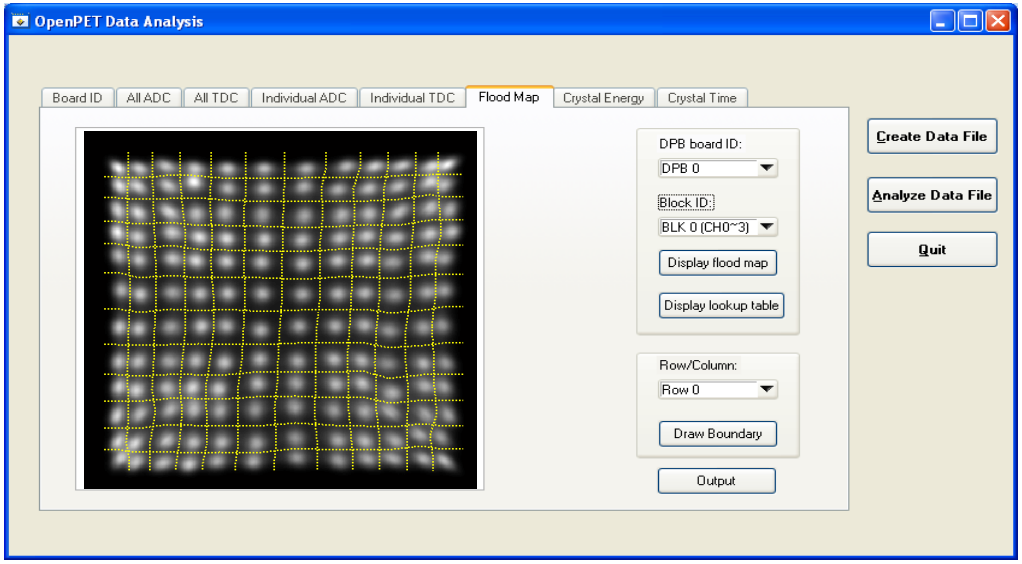
We will provide Hardware Abstract Layer (HAL) API.

We will implement a JTAG debug module in the μ-processor. So you will be able to debug (set break point, single step, check/set variable value and etc.) on-line using an Altera USB-blaster download cable

PC Software

- **Design Software: NI LabWindows/CVI 9.0 ($2,599)**
- **Design Language: Standard C**

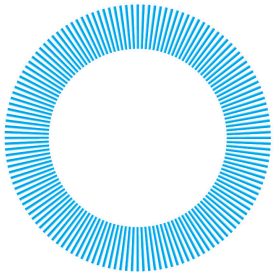




We will provide lower-level data communication API for both high-speed data buffering and low-speed data/command communications.

Schedule

- **Circuit Board Schedule**
  - **Board design complete** — **Mid Dec.**
  - **Board fabrication complete** — **Mid Jan.**
  - **Board integration begins** — **End Jan.**
- **Boards Available to Users (limited software)** — **February**



openPET

the open source, standardized, nuclear medical electronics system

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